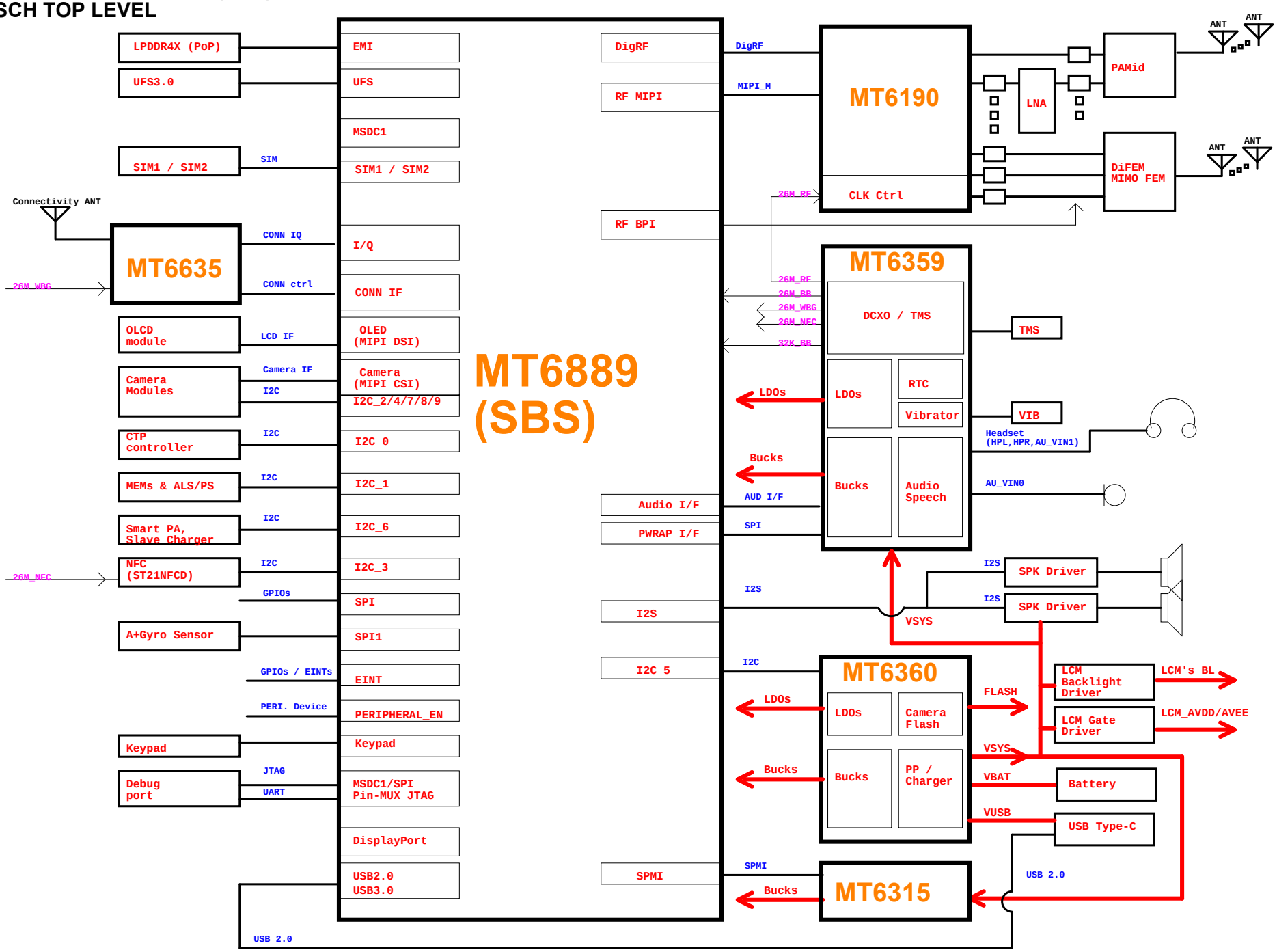
Project : MT6889, LPDDR4X (SBS)
REF_SCH TOP LEVEL



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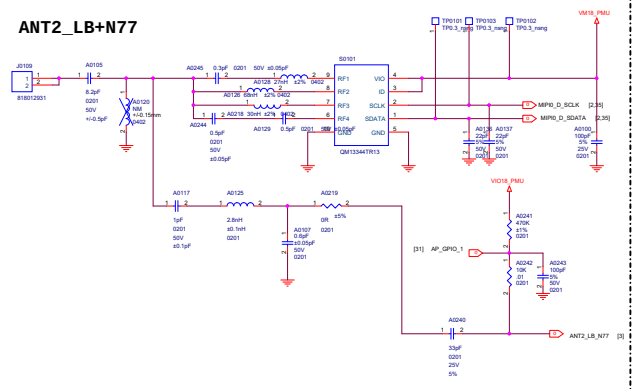
Size C	Document Number Diagram	Rev P0
Date: Thursday, August 26, 2021	Sheet	

ANT2_LB+N77



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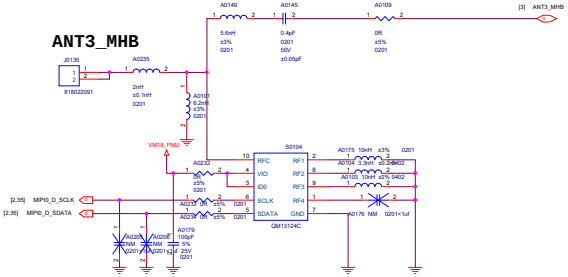
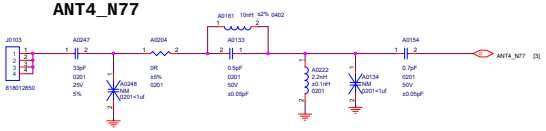
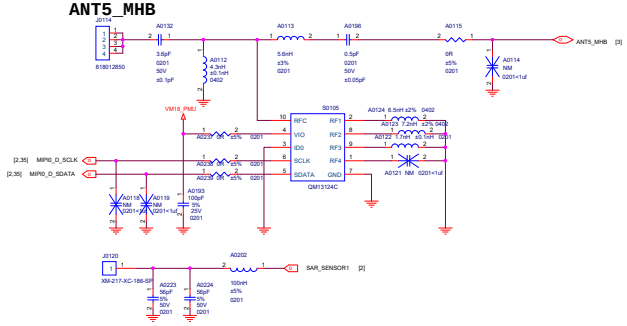


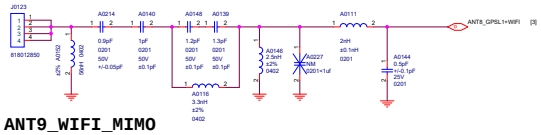
ANT4_N77



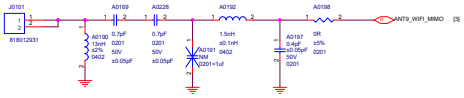
ANT5_MHB



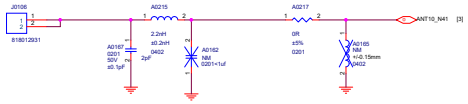
ANT8_GPSL1+WIFI



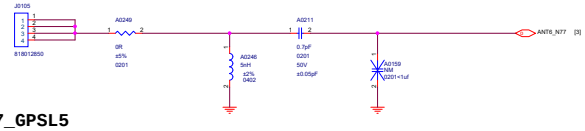
ANT9_WIFI_MIMO



ANT10_N41



ANT6_N77



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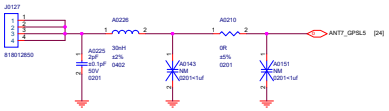
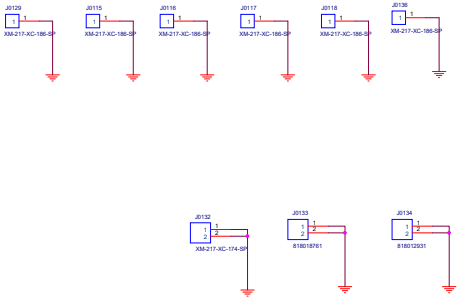
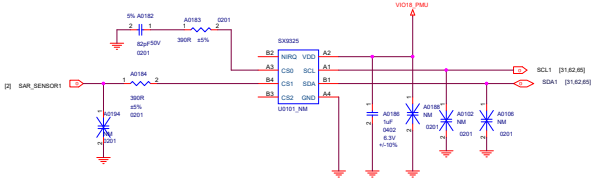


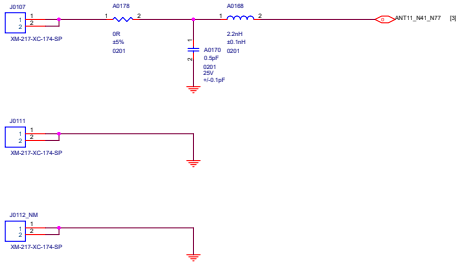
MAIN PCB GND



SAR Sensor



ANT11_N41_N77



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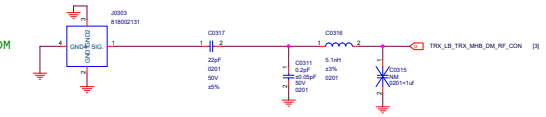
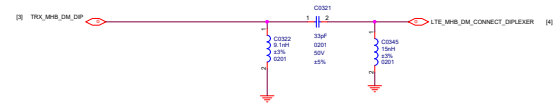
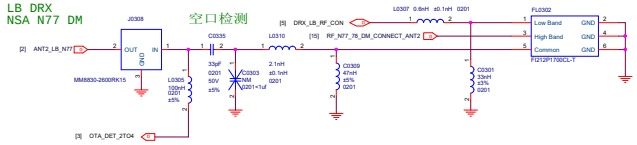
LTE MHB_DRX_MIMO
SA/NSA N1/N3/N41 DM
N77/78 DRX MIMO

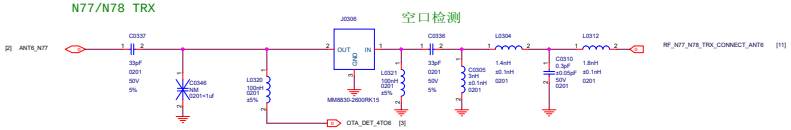




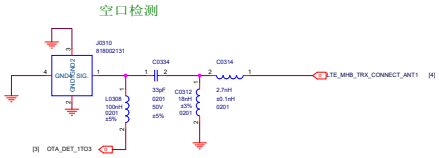
ANT2
LB DRX
NSA N77 DM



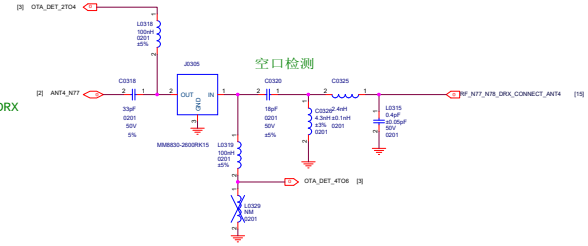
ANT6
N77/N78 TRX



ANT1
MHB TRX
SA N1/N3/N41 TRX
NSA N1/N3/N41 TRX



ANT4
N77/N78 DRX



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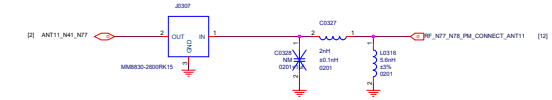
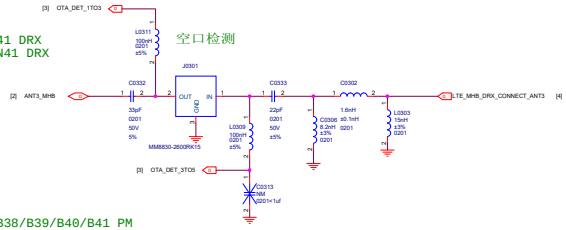
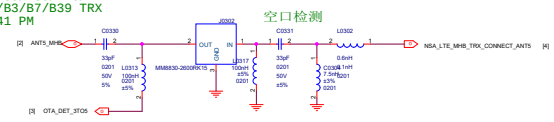
N77/N78 PM



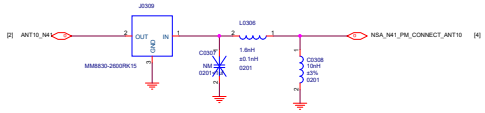
ANT3
MHB DRX
SA N1/N3/N41 DRX
NSA N1/N3/N41 DRX



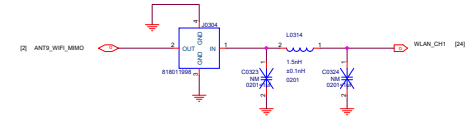
ANT5
LTE B1/B3/B38/B39/B40/B41 PM
NSA LTE B1/B3/B7/B39 TRX
SA N1/N3/N41 PM



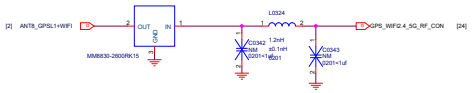
ANT10
NSA N41 PM



ANT9
WIFI1



ANT8
GPSL1+WIFI



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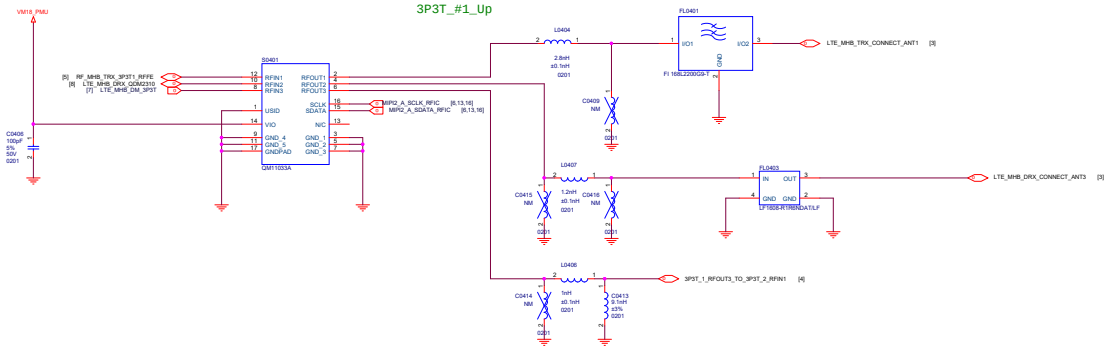

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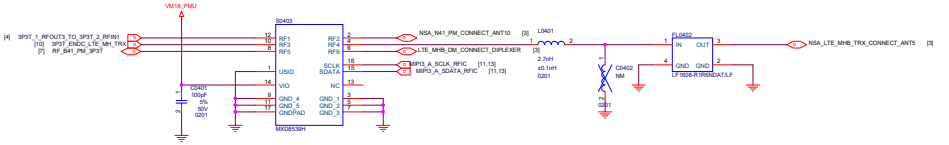
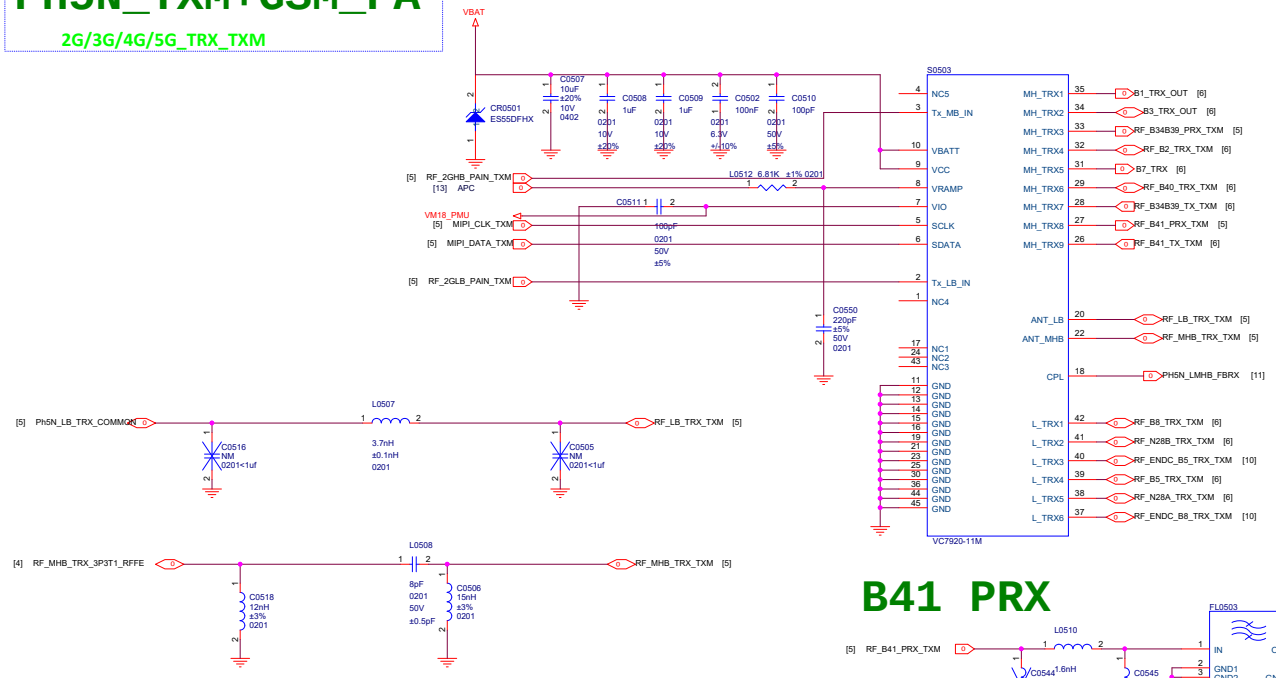
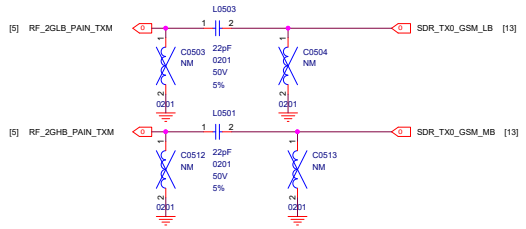


Ph5N_TXM+GSM_PA

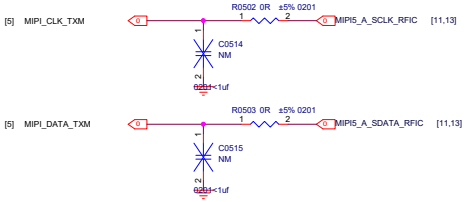
2G/3G/4G/5G_TRX_TXM



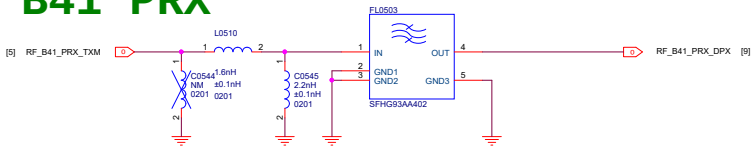
GSM PA_IN MATCH



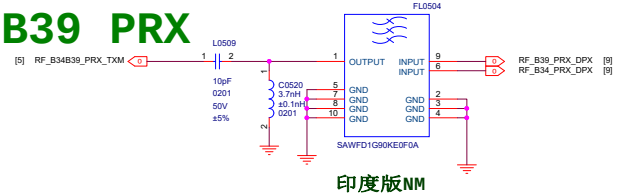
TXM MIPI CTRL



B41 PRX

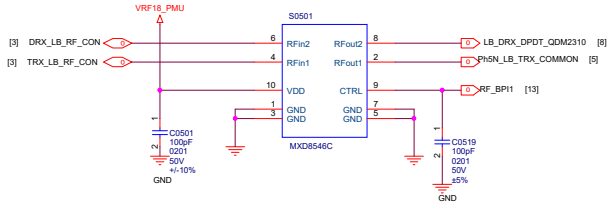


B34 B39 PRX



印度版NM

LB TAS DPDT



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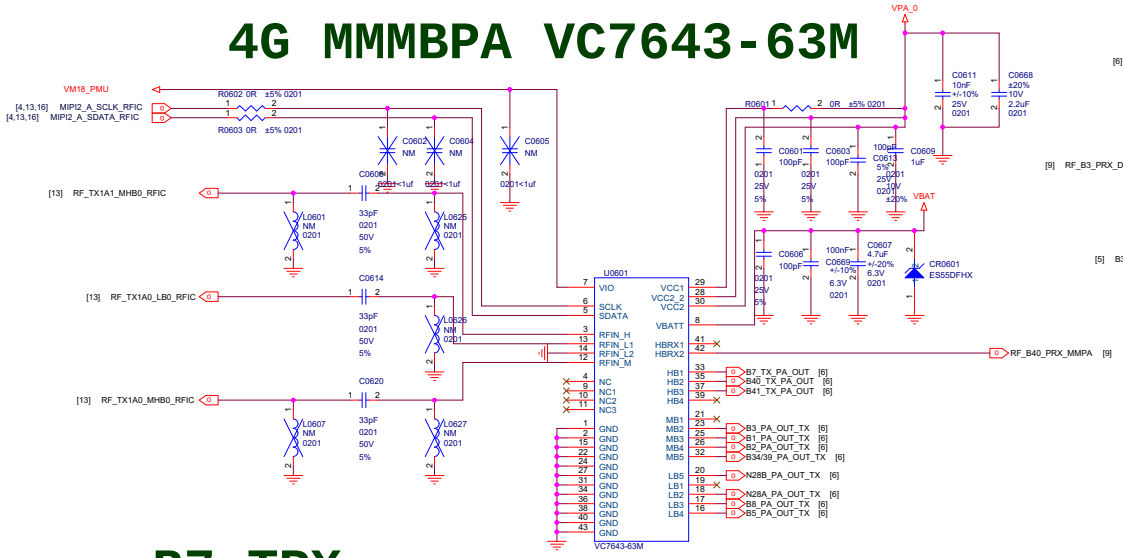
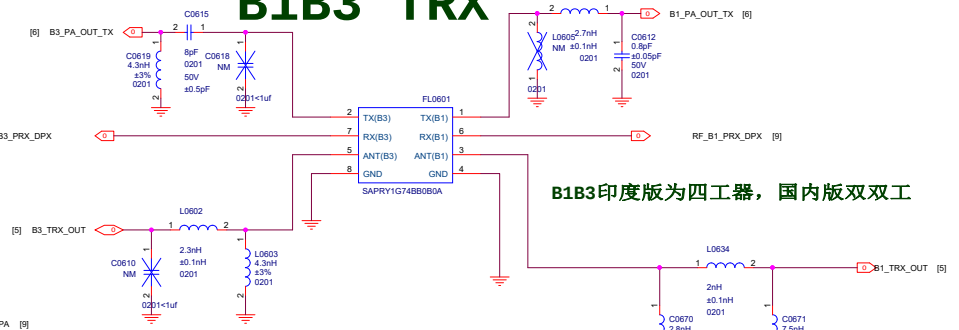
Size	Document Number	Rev
A2	MT6893_GPIO_1	
Date:	Sheet	

Thursday, August 26, 2021

4G MMMBPA VC7643-63M

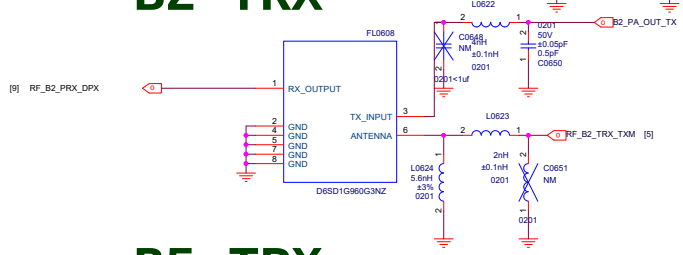


B1B3 TRX

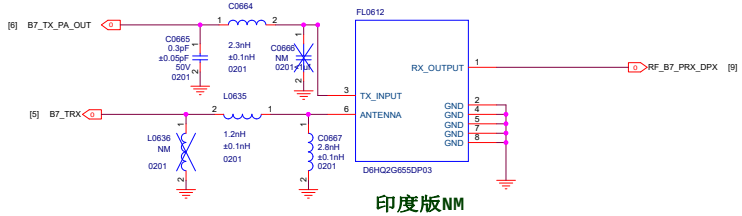


B1B3印度版为四工器，国内版双双工

B2 TRX

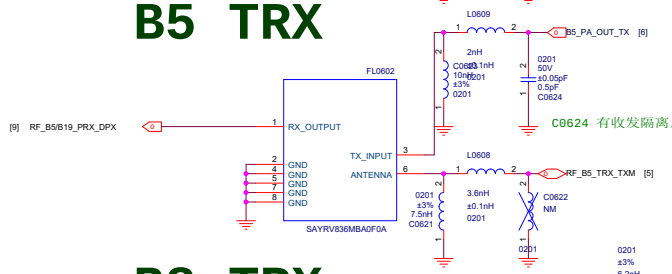


B7 TRX



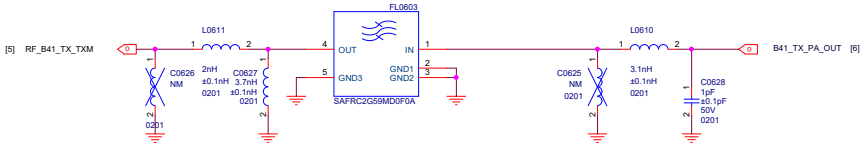
印度版NM

B5 TRX

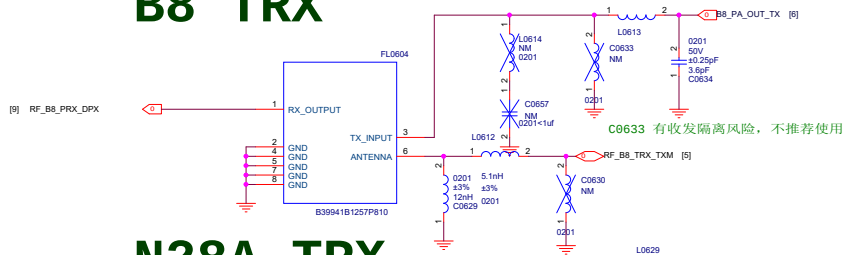


C0624 有收发隔离风险，不推荐使用

B38/B41 TX

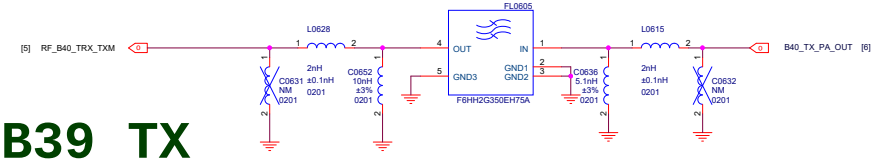


B8 TRX

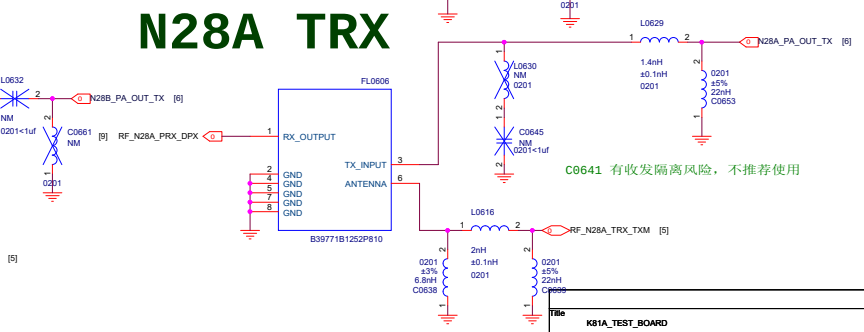


C0633 有收发隔离风险，不推荐使用

B40 TRX

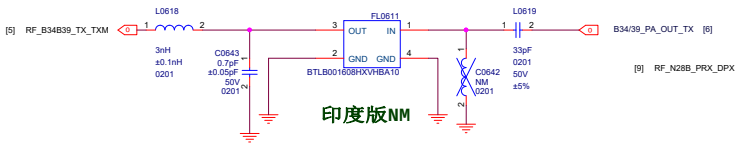


N28A TRX



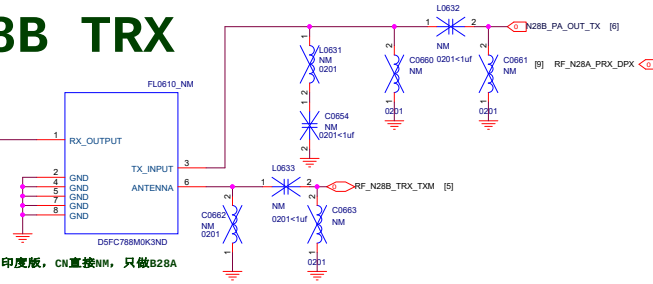
C0641 有收发隔离风险，不推荐使用

B34/B39 TX



印度版NM

N28B TRX



SPDT 与B28B的双工为印度版，CN直接NM，只做B28A

Title	K81A_TEST_BOARD	
Size A2	Document Number PM8655B Charger	Rev P0
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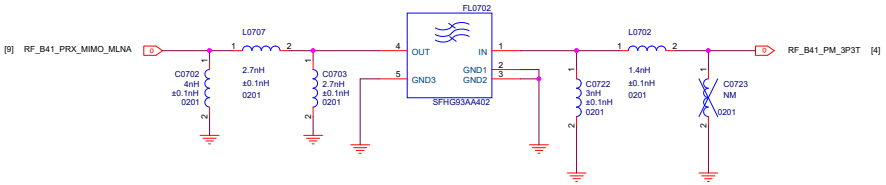
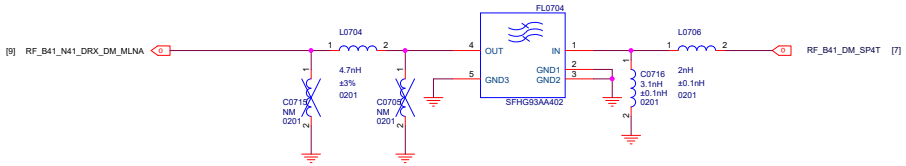
* * * * * * * * * * * * *PRX MIMO* * * * * * * * * * * * * * *

B41 PRX MIMO

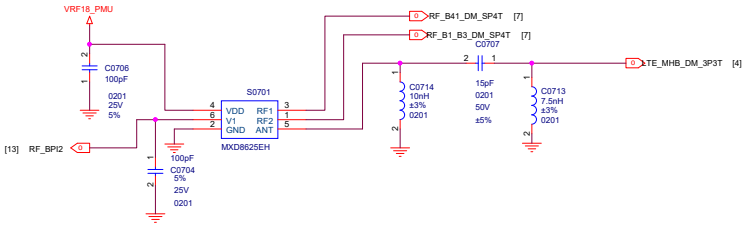


* * * * * * * * * * * * *DRX MIMO* * * * * * * * * * * * * * *

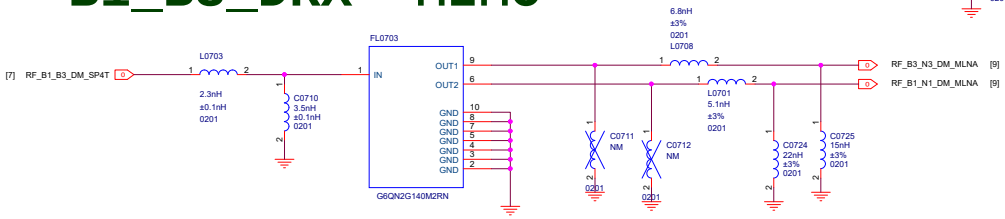
B41 DRX MIMO CN
B40 RX SAW INDIA



CN为B41 RX SAW,印度为B40 RX SAW



B1_B3_DRX MIMO



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Size A2	Document Number PM8550B Charger	Rev P0
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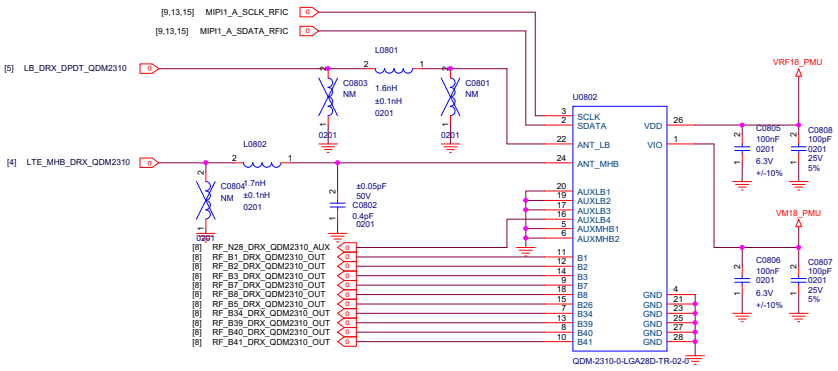
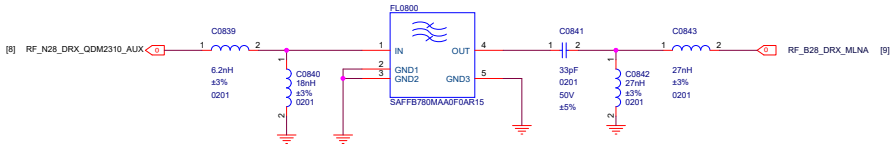
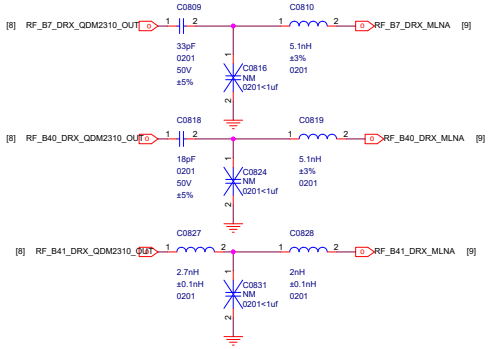
DiFEM QDM2310



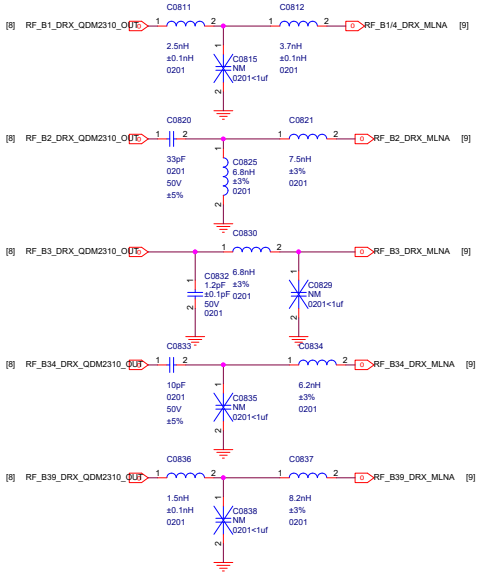
N28 DRX



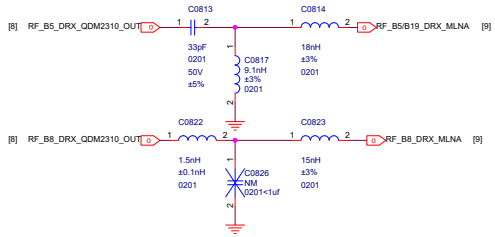
DRX HB



DRX MB



DRX LB



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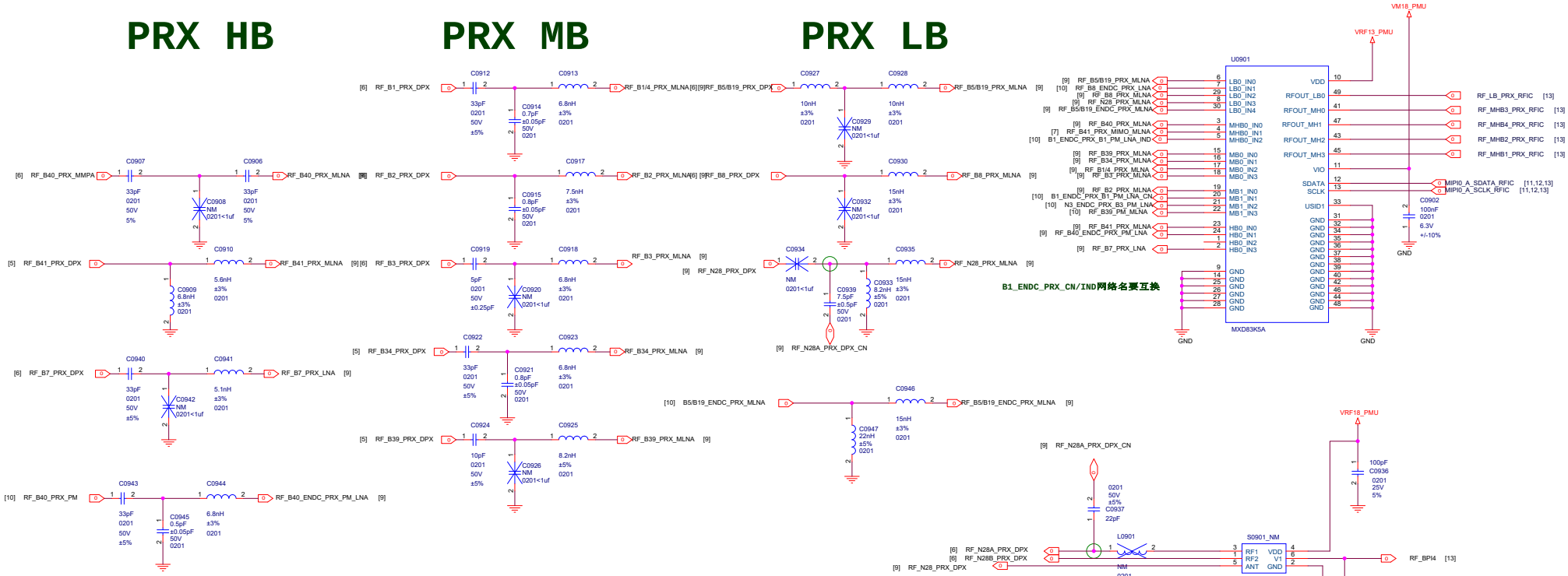
PRX LNA-Bank MXD83K5A Matching

PRX HB

PRX MB

PRX LB

MHB PRX



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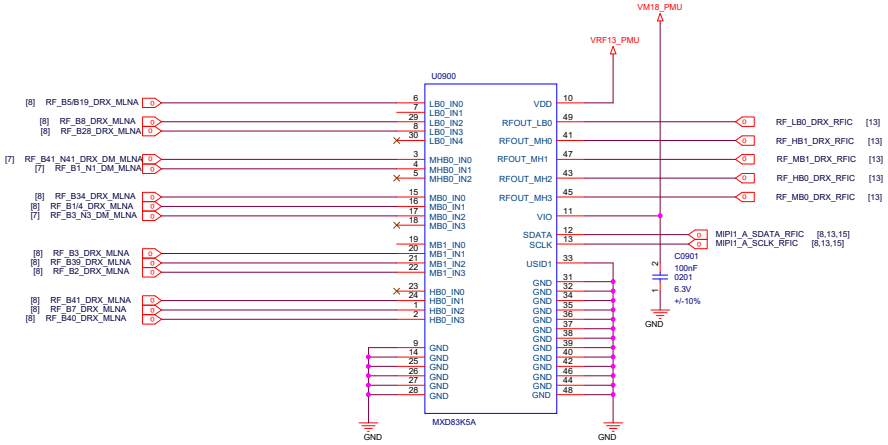

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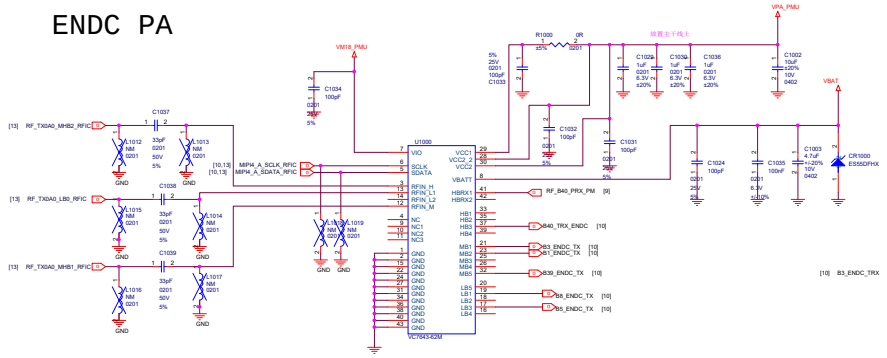
ENDC PA



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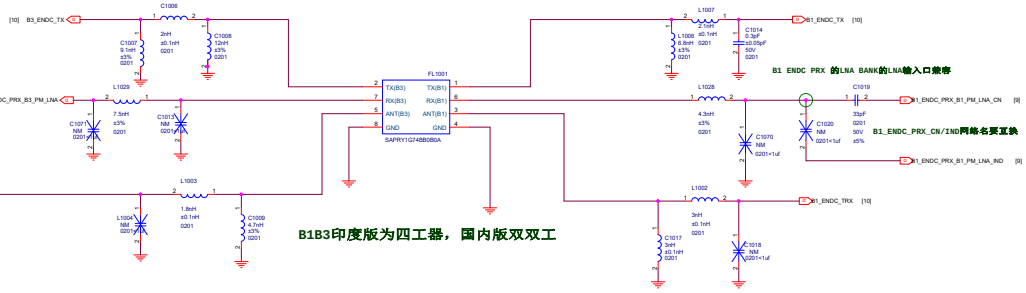
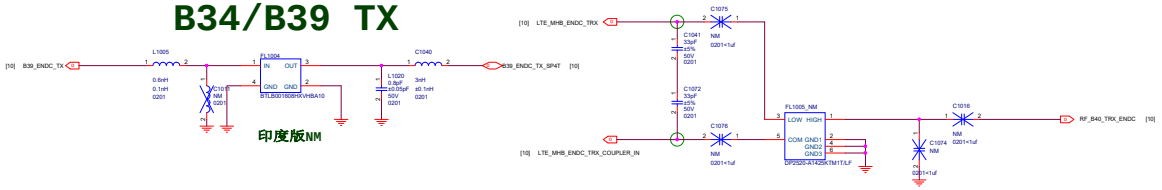
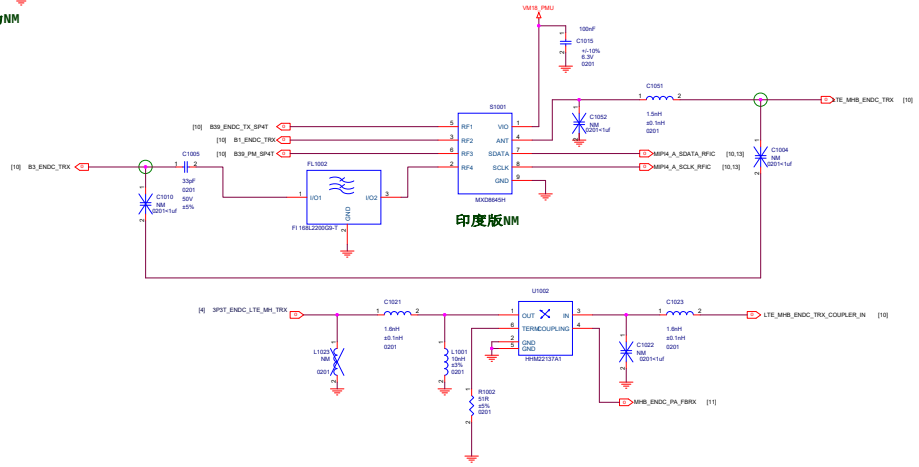
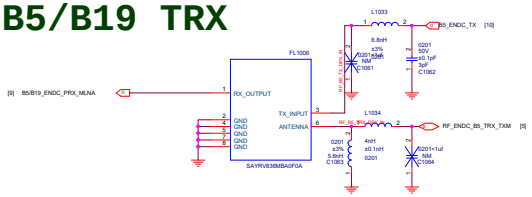


B34/B39 TX

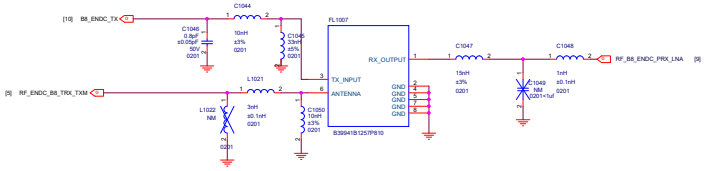




B5/B19 TRX



B8 TRX



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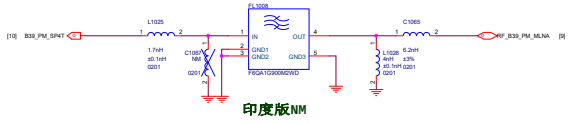
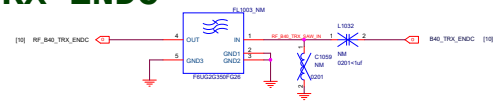
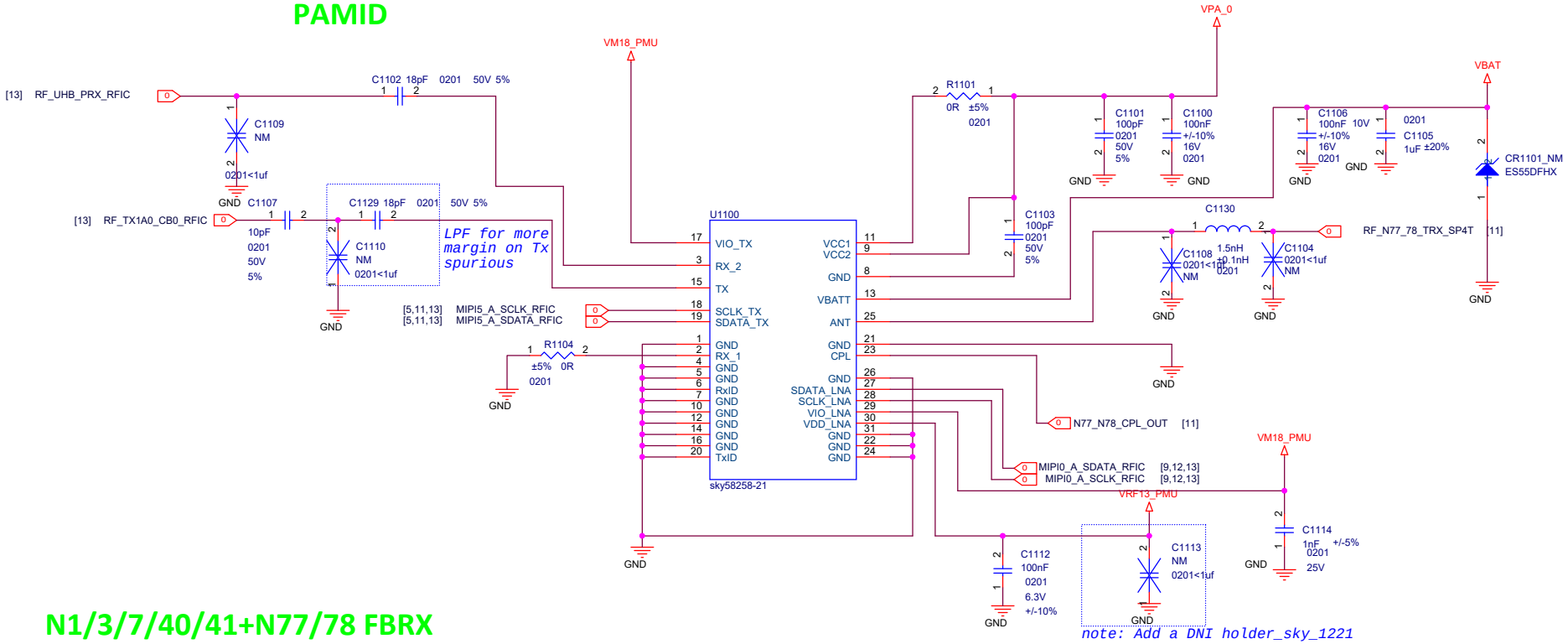


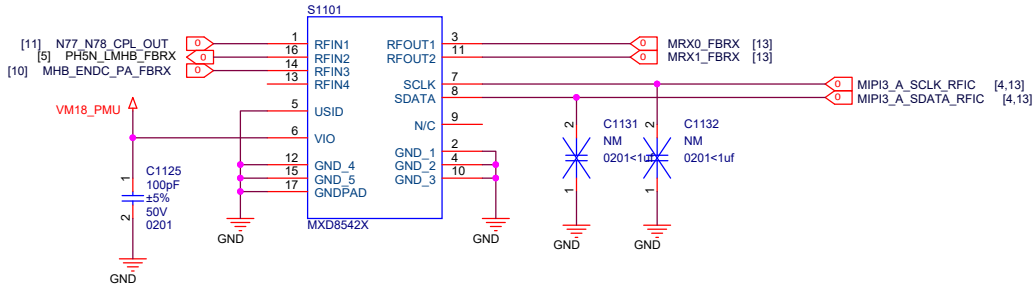
B40 TRX ENDC

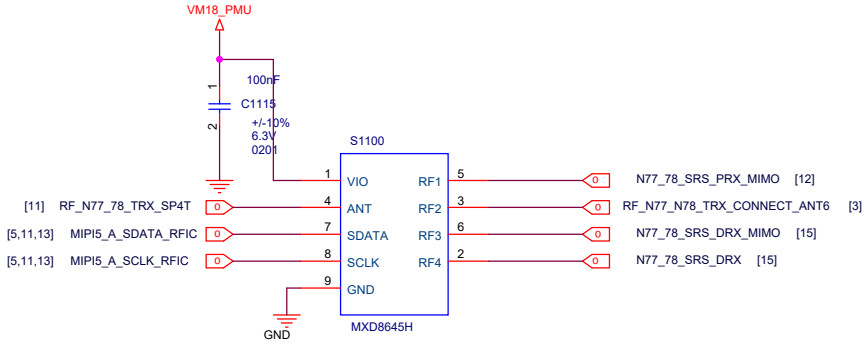


NR N77/N78 PAMID



N1/3/7/40/41+N77/78 FBRX





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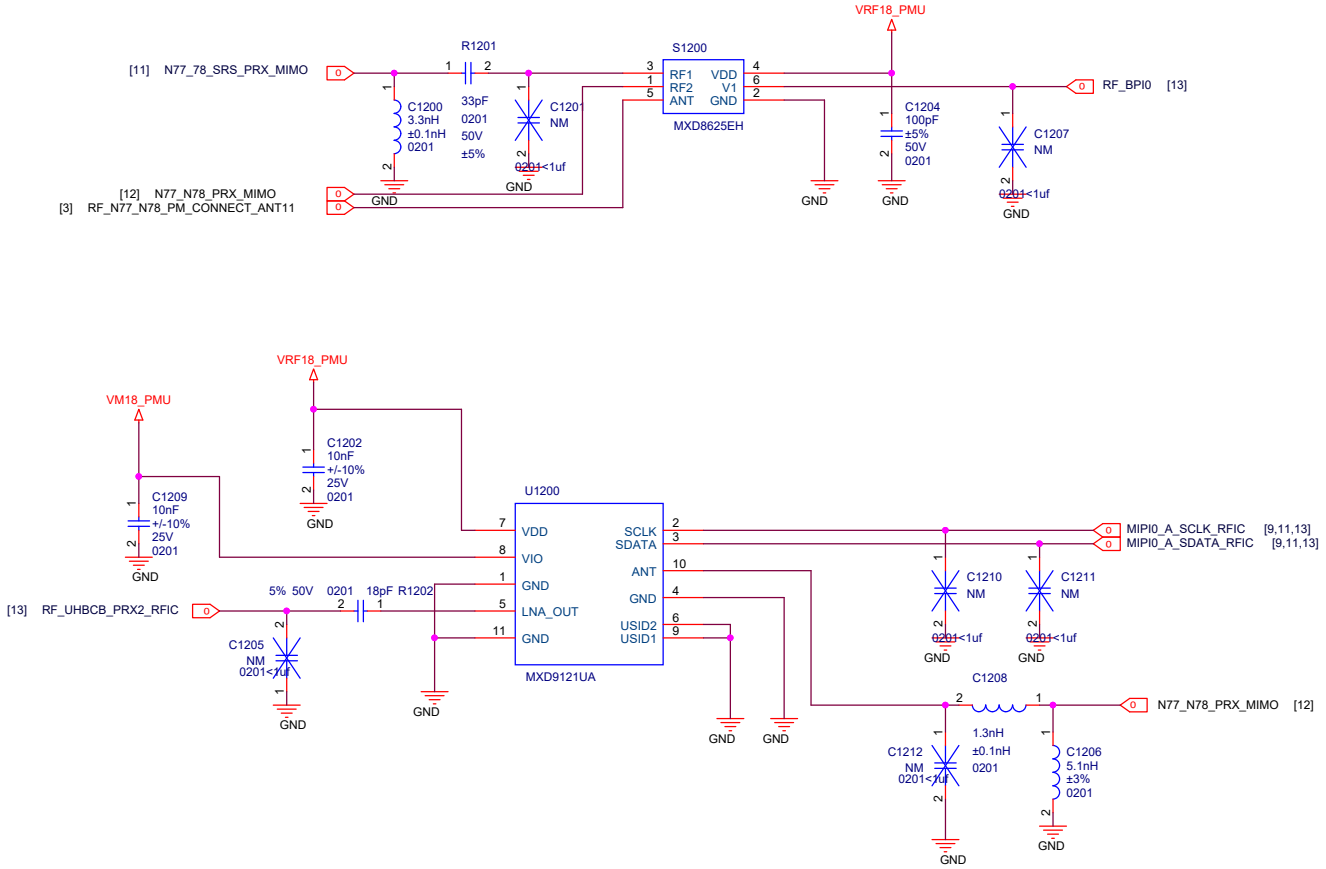
NR N77/N78 PRx-MIMO LFEM



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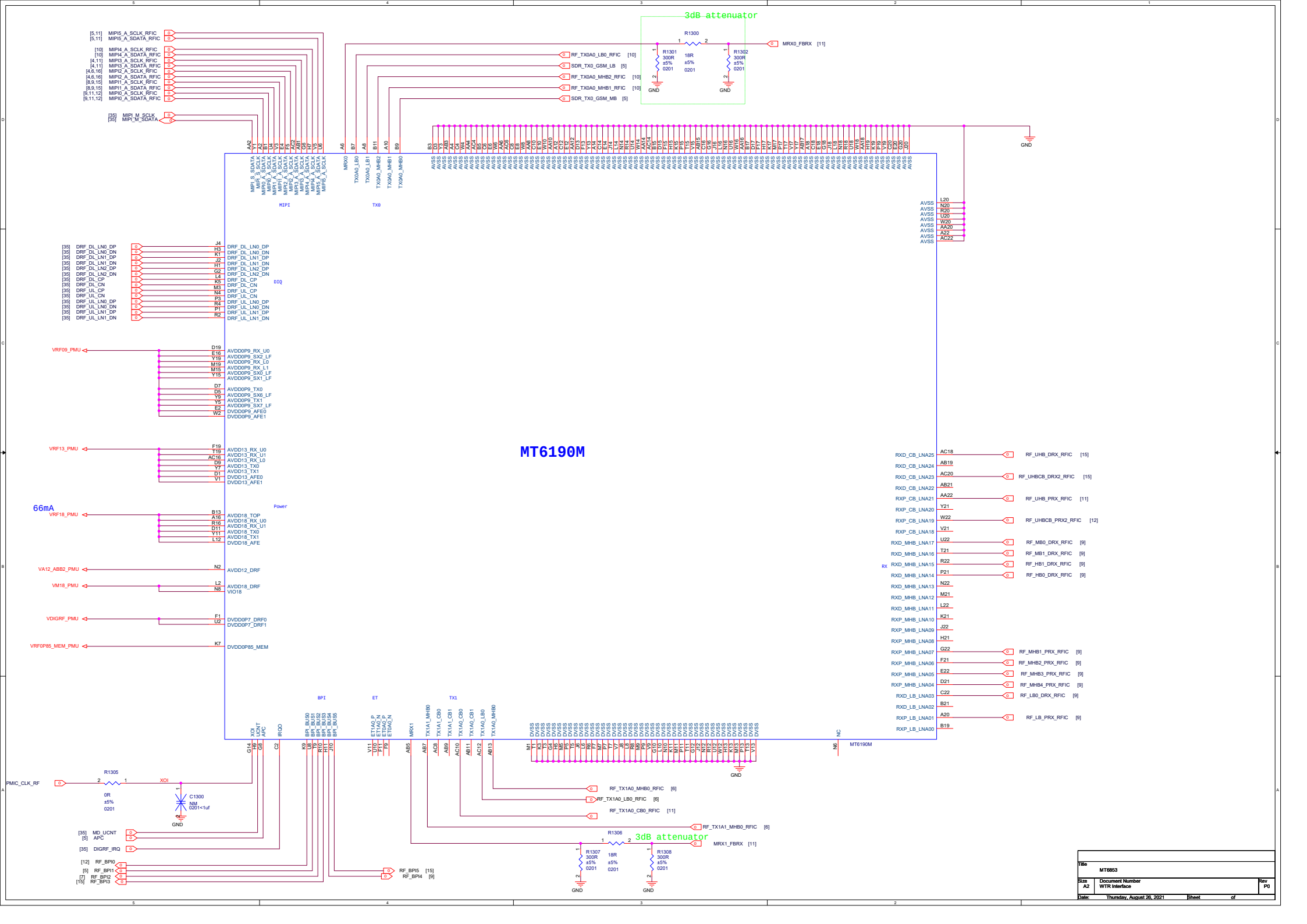
MT6190M
3dB attenuator
R1300
R1301
300R
±5%
0201
18R
±5%
0201
R1302
300R
±5%
0201
MRX0_FBRX [11]
RF_TX0A0_LB0_RFIC [10]
SDR_TX0_GSM_LB [5]
RF_TX0A0_MHB2_RFIC [10]
RF_TX0A0_MHB1_RFIC [10]
SDR_TX0_GSM_MB [5]
[5,11] MIPI5_A_SCLK_RFIC
[5,11] MIPI5_A_SDATA_RFIC
[10] MIPI4_A_SCLK_RFIC
[10] MIPI4_A_SDATA_RFIC
[4,11] MIPI3_A_SCLK_RFIC
[4,11] MIPI3_A_SDATA_RFIC
[4,6,16] MIPI2_A_SCLK_RFIC
[4,6,16] MIPI2_A_SDATA_RFIC
[8,9,15] MIPI1_A_SCLK_RFIC
[8,9,15] MIPI1_A_SDATA_RFIC
[9,11,12] MIPI0_A_SCLK_RFIC
[9,11,12] MIPI0_A_SDATA_RFIC
[35] MIPI_M_SCLK
[35] MIPI_M_SDATA
MIPI
TX0
DIQ
Power
BPI
ET
TX1
[35] DRF_DL_LN0_DP
[35] DRF_DL_LN0_DN
[35] DRF_DL_LN1_DP
[35] DRF_DL_LN1_DN
[35] DRF_DL_LN2_DP
[35] DRF_DL_LN2_DN
[35] DRF_DL_CP
[35] DRF_DL_CN
[35] DRF_UL_CP
[35] DRF_UL_CN
[35] DRF_UL_LN0_DP
[35] DRF_UL_LN0_DN
[35] DRF_UL_LN1_DP
[35] DRF_UL_LN1_DN
VRF09_PMU
VRF13_PMU
66mA
VRF18_PMU
VA12_ABB2_PMU
VM18_PMU
VDIGRF_PMU
VRF0P85_MEM_PMU
RXD_CB_LNA25
RXD_CB_LNA24
RXD_CB_LNA23
RXD_CB_LNA22
RXP_CB_LNA21
RXP_CB_LNA20
RXP_CB_LNA19
RXP_CB_LNA18
RXD_MHB_LNA17
RXD_MHB_LNA16
RXD_MHB_LNA15
RXD_MHB_LNA14
RXD_MHB_LNA13
RXD_MHB_LNA12
RXD_MHB_LNA11
RXP_MHB_LNA10
RXP_MHB_LNA09
RXP_MHB_LNA08
RXP_MHB_LNA07
RXP_MHB_LNA06
RXP_MHB_LNA05
RXP_MHB_LNA04
RXD_LB_LNA03
RXD_LB_LNA02
RXP_LB_LNA01
RXP_LB_LNA00
RX
RF_UHB_DRX_RFIC [15]
RF_UHBCB_DRX2_RFIC [15]
RF_UHB_PRX_RFIC [11]
RF_UHBCB_PRX2_RFIC [12]
RF_MB0_DRX_RFIC [9]
RF_MB1_DRX_RFIC [9]
RF_HB1_DRX_RFIC [9]
RF_HB0_DRX_RFIC [9]
RF_MHB1_PRX_RFIC [9]
RF_MHB2_PRX_RFIC [9]
RF_MHB3_PRX_RFIC [9]
RF_MHB4_PRX_RFIC [9]
RF_LB0_DRX_RFIC [9]
RF_LB_PRX_RFIC [9]
PMIC_CLK_RF
R1305
0R
±5%
0201
XOI
C1300
NM
0201<1uf
[35] MD_UCNT
[5] APC
[35] DIGRF_IRQ
[12] RF_BPI0
[5] RF_BPI1
[7] RF_BPI2
[15] RF_BPI3
RF_BPI5 [15]
RF_BPI4 [9]
RF_TX1A0_MHB0_RFIC [6]
RF_TX1A0_LB0_RFIC [6]
RF_TX1A0_CB0_RFIC [11]
RF_TX1A1_MHB0_RFIC [6]
R1306
3dB attenuator
MRX1_FBRX [11]
R1307
300R
±5%
0201
18R
±5%
0201
R1308
300R
±5%
0201
GND
Title
MT6853
Size
A2
Document Number
WTR Interface
Rev
P0
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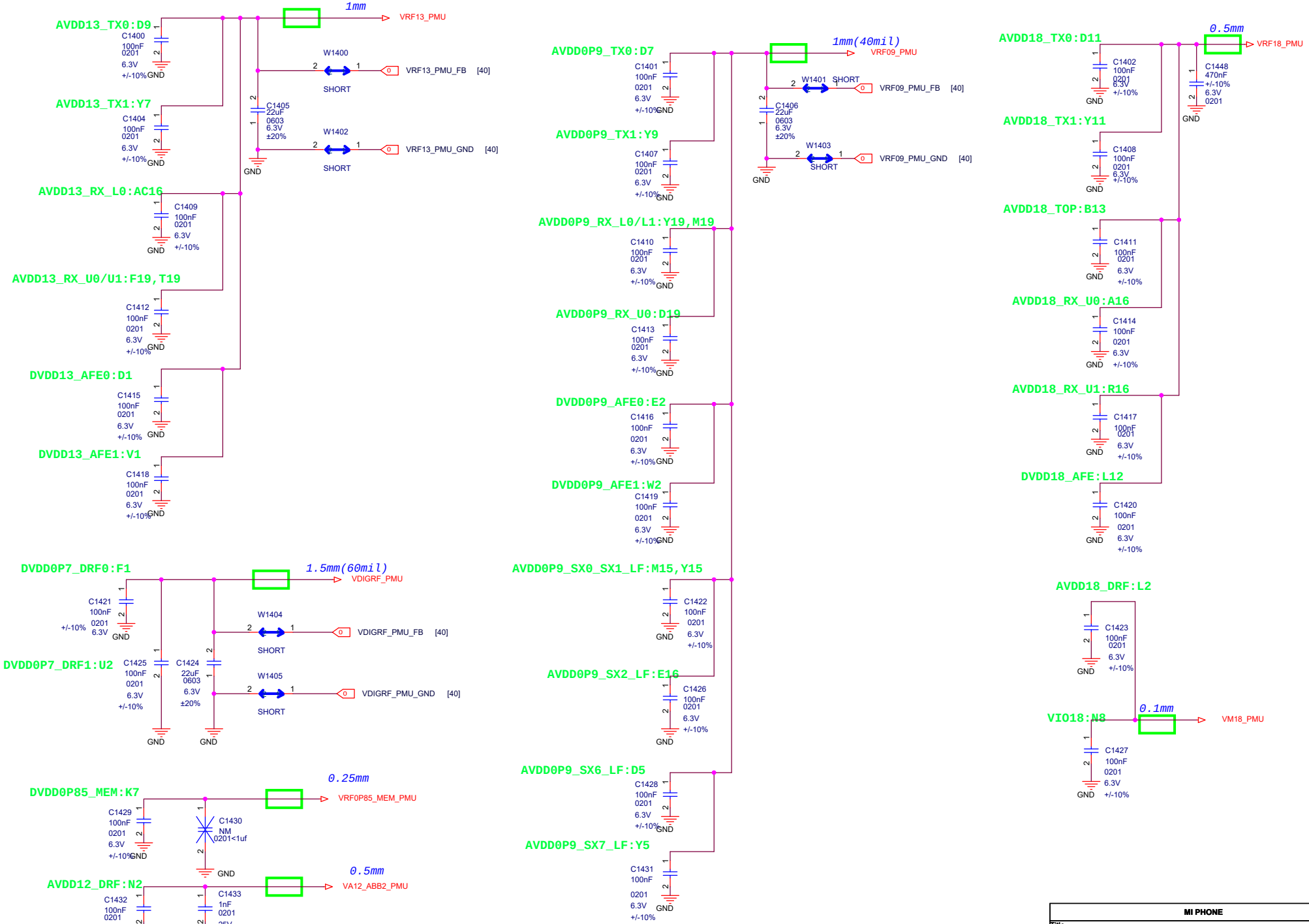
of



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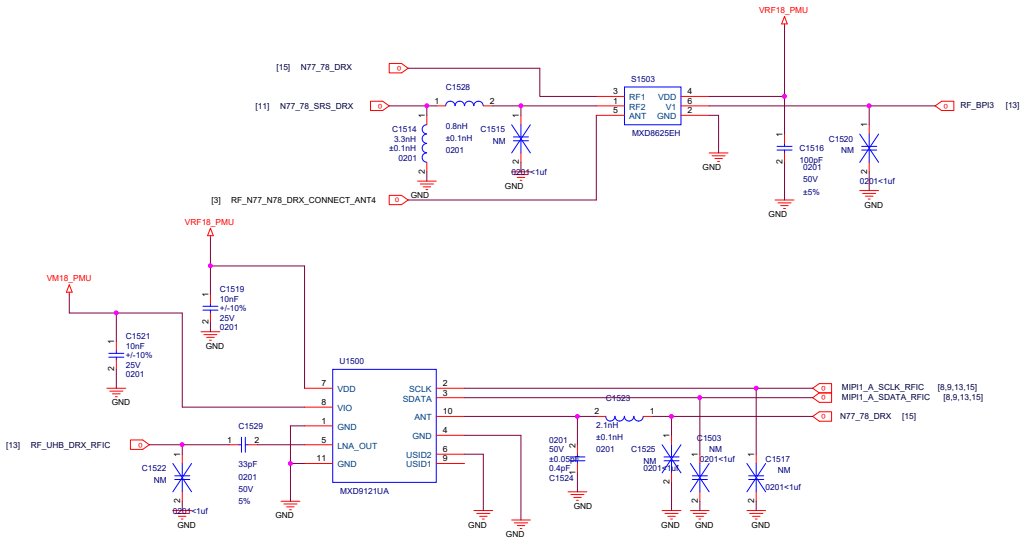
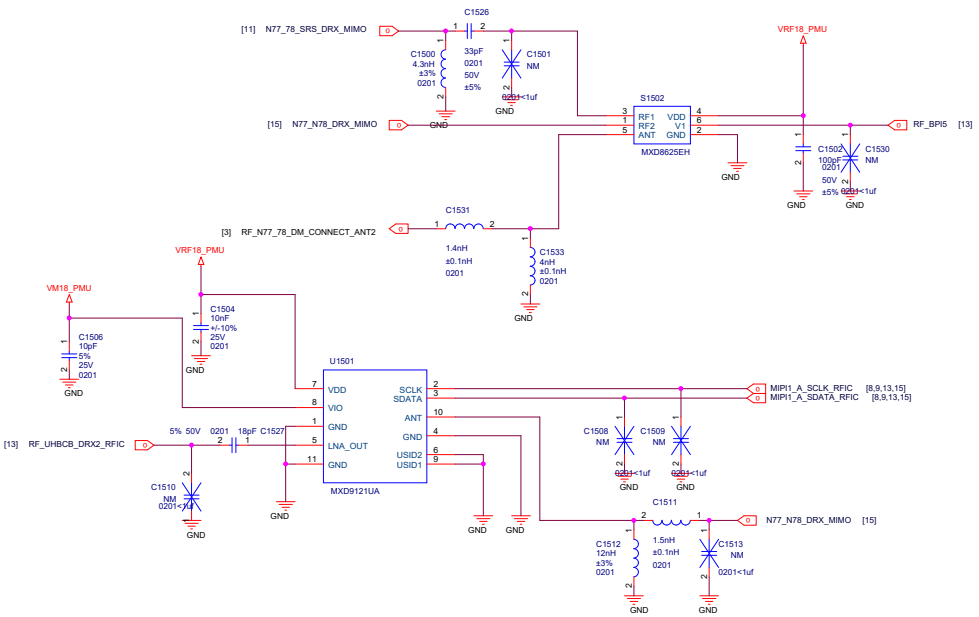
NR N77/N78/N79 DRx-LFEM



NR N77/N78/N79 DRx_MIMO-LFEM



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Size A2	Document Number 5G_MIMO_LNA		Rev P0
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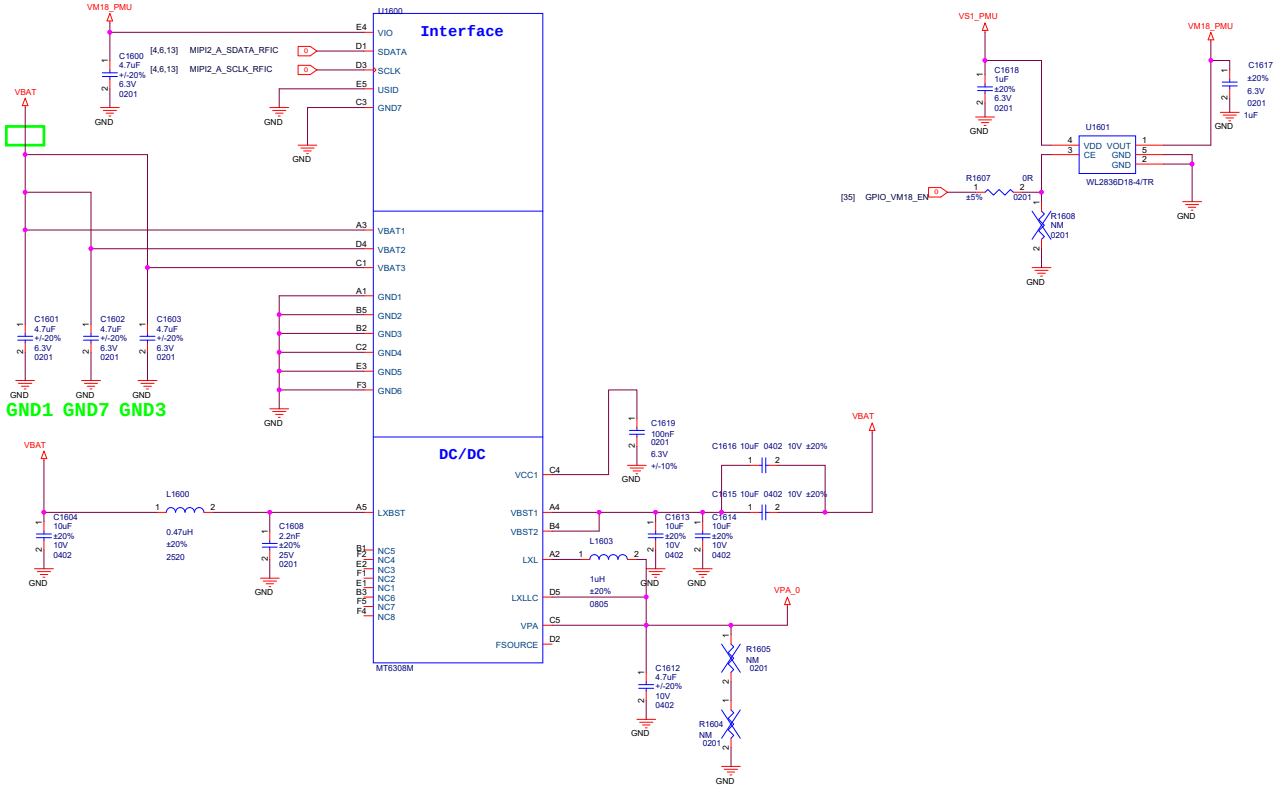
PH5N_N77_PA_电源



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Title K16_MAIN		
Size A3	Document Number Reserved(for 5G-sub 6G)	Rev P0
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Size A3	Document Number Reserved(for 5G-sub 6G)	Rev P0
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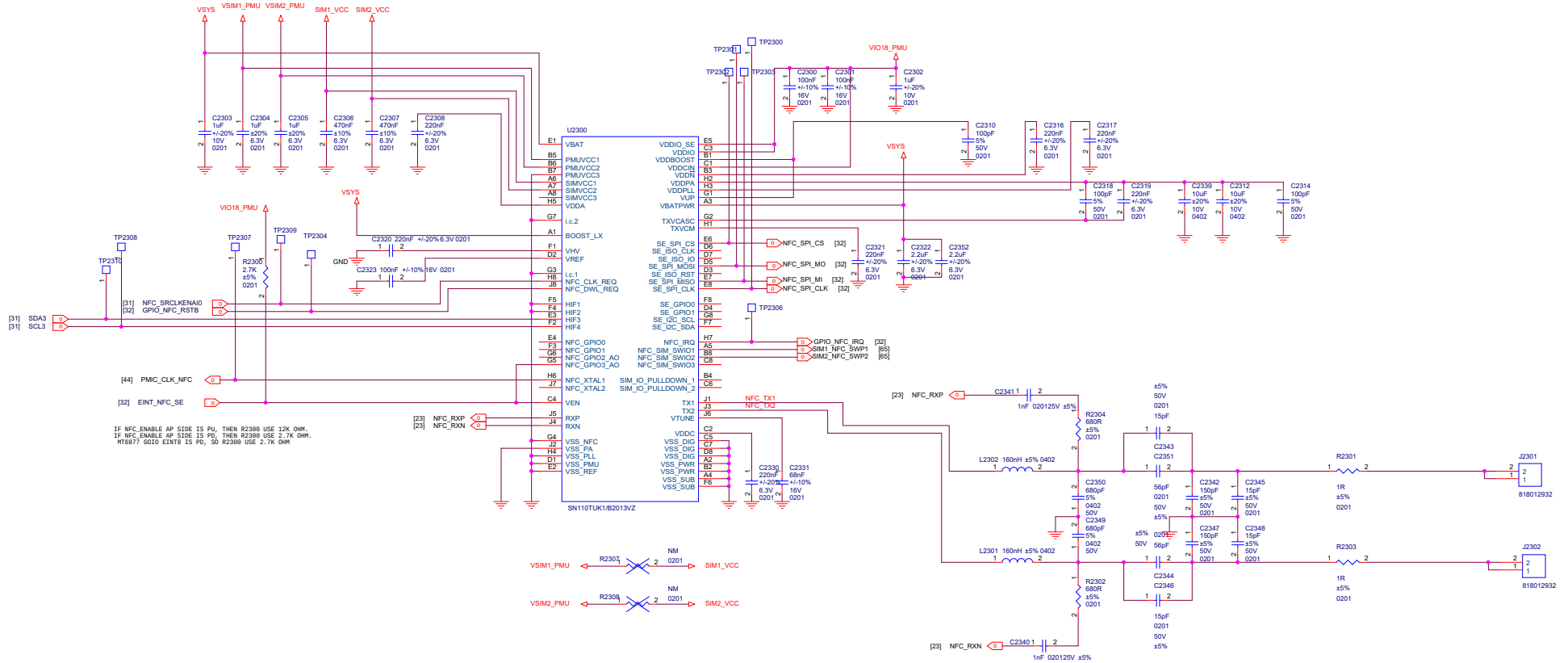

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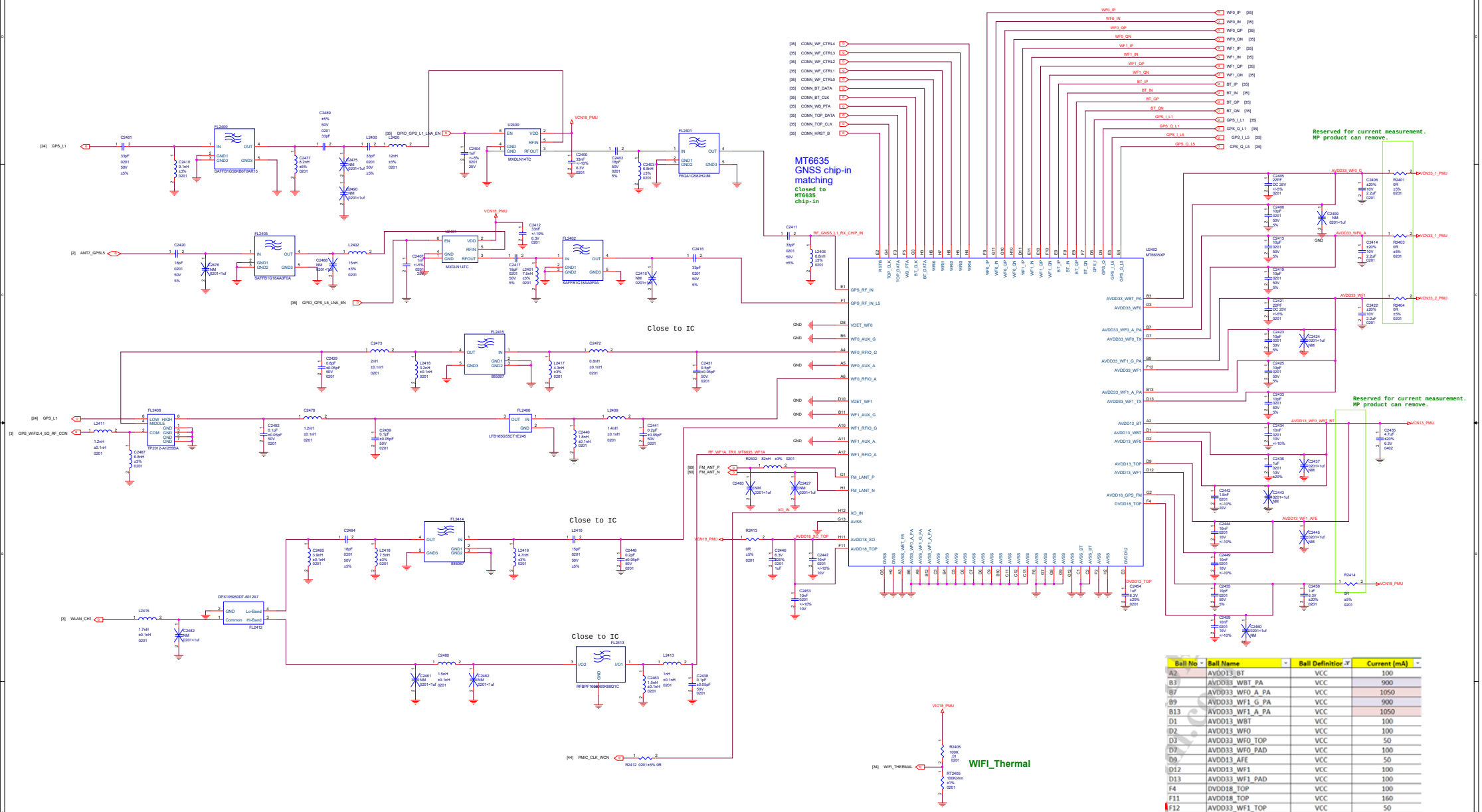

Ball No	Ball Name	Ball Definition	Current (mA)
A2	AVDD13_BT	VCC	100
B3	AVDD33_WBT_PA	VCC	900
B7	AVDD33_WF0_A_PA	VCC	1050
B9	AVDD33_WF1_G_PA	VCC	900
B13	AVDD33_WF1_A_PA	VCC	1050
D1	AVDD13_WBT	VCC	100
D2	AVDD13_WF0	VCC	100
D3	AVDD33_WF0_TOP	VCC	50
D7	AVDD33_WF0_PAD	VCC	100
D9	AVDD13_AFE	VCC	50
D12	AVDD13_WF1	VCC	100
D13	AVDD33_WF1_PAD	VCC	100
F4	DVDD18_TOP	VCC	100
F11	AVDD18_TOP	VCC	160
F12	AVDD33_WF1_TOP	VCC	50
G2	AVDD18_GPS_FM	VCC	50
H11	AVDD18_XO	VCC	10

MI PHONE		
Title: MT6873_5GA		
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MI PHONE		
Title MT6873_5GA		
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MI PHONE		
Title: MT6873_5GA		
Size: A3	Document Number: Reserved(for 11ad/11ax)	Rev: P0
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MI PHONE		
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MI PHONE		
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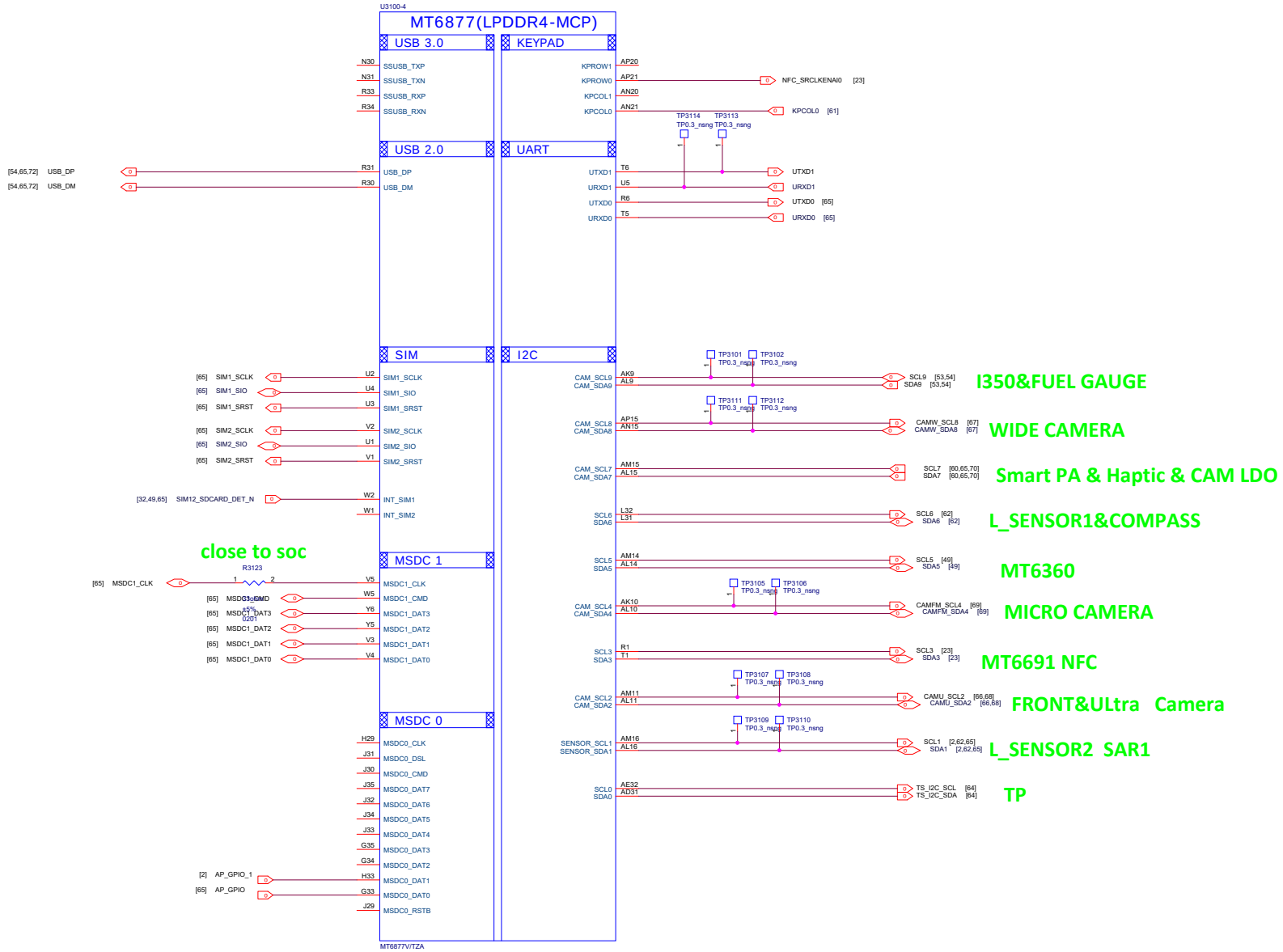

Title	MT6877 GPIO-1	
Size A2	Document Number MT6877	Rev P0
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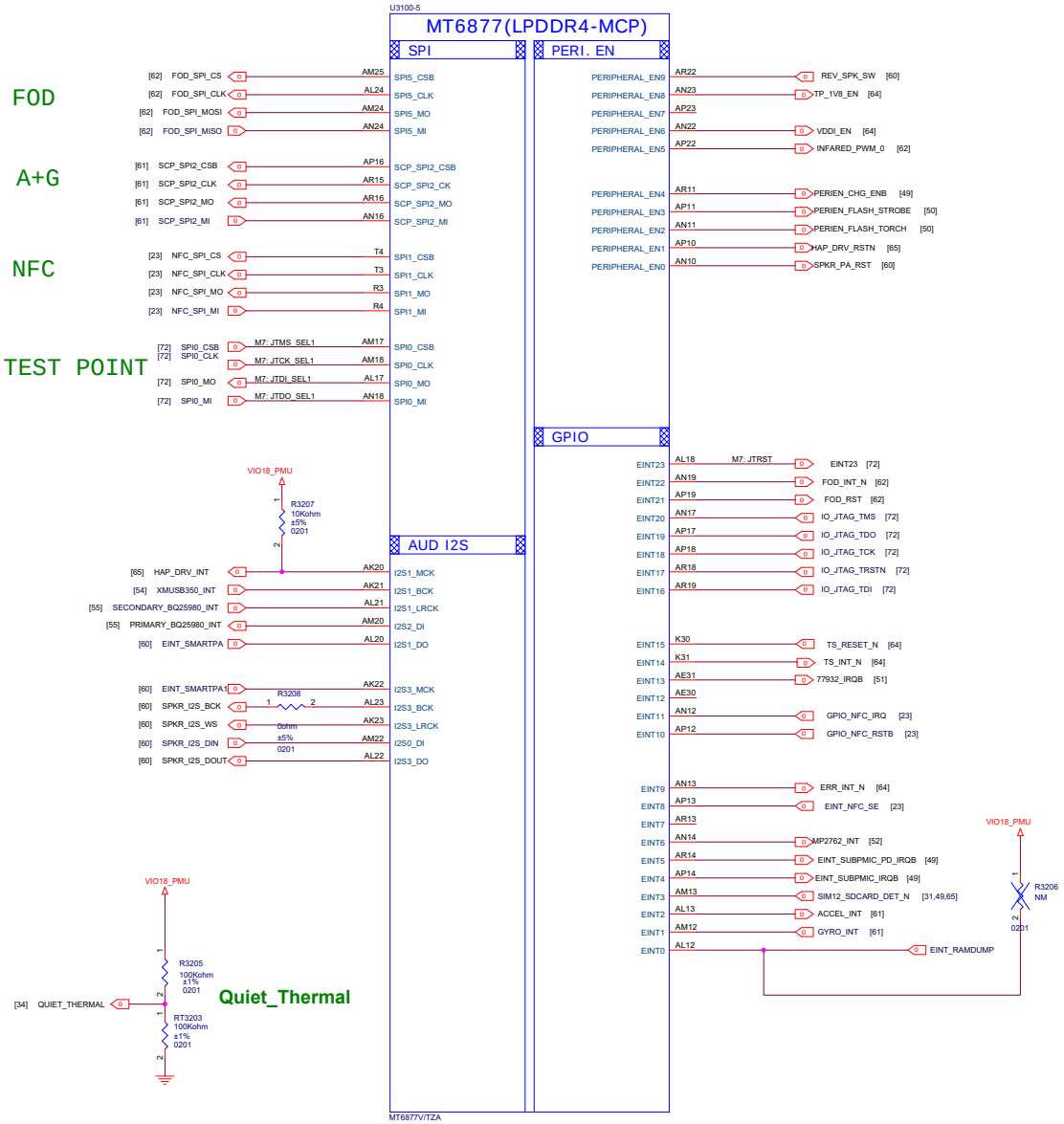

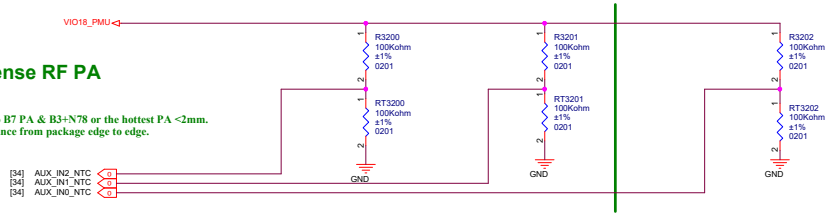

Thermistor to sense RF PA temperature

1. RT3200 & RT3201 must close to B7 PA & B3+N78 or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

Thermistor to sense AP temperature

1. RT3202 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

Title	MT6877 GPIO-2	
Size A2	Document Number MT6877	Rev P0
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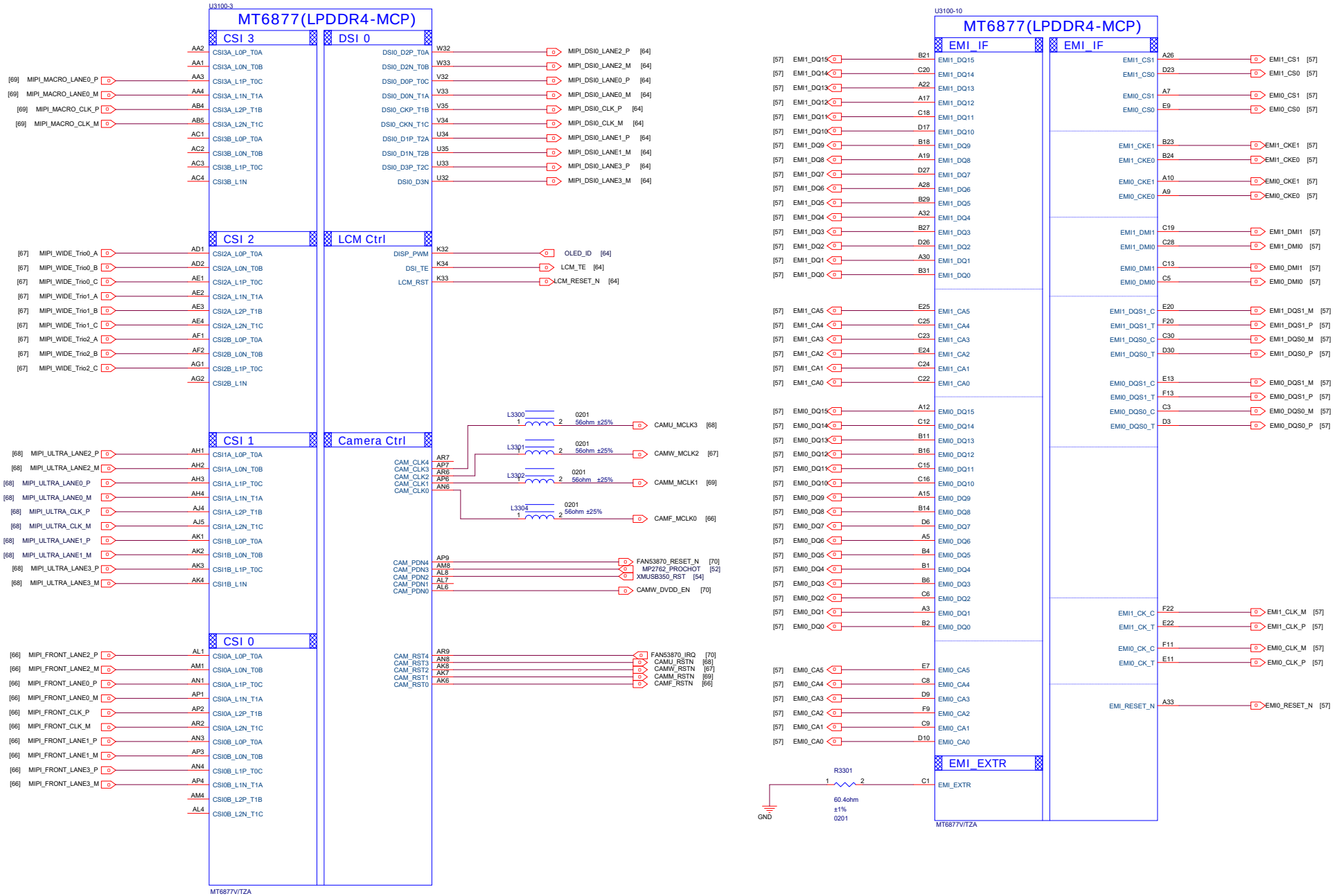

Title	MT6877 CAM LCM EMI
Size C	Document Number MT6877
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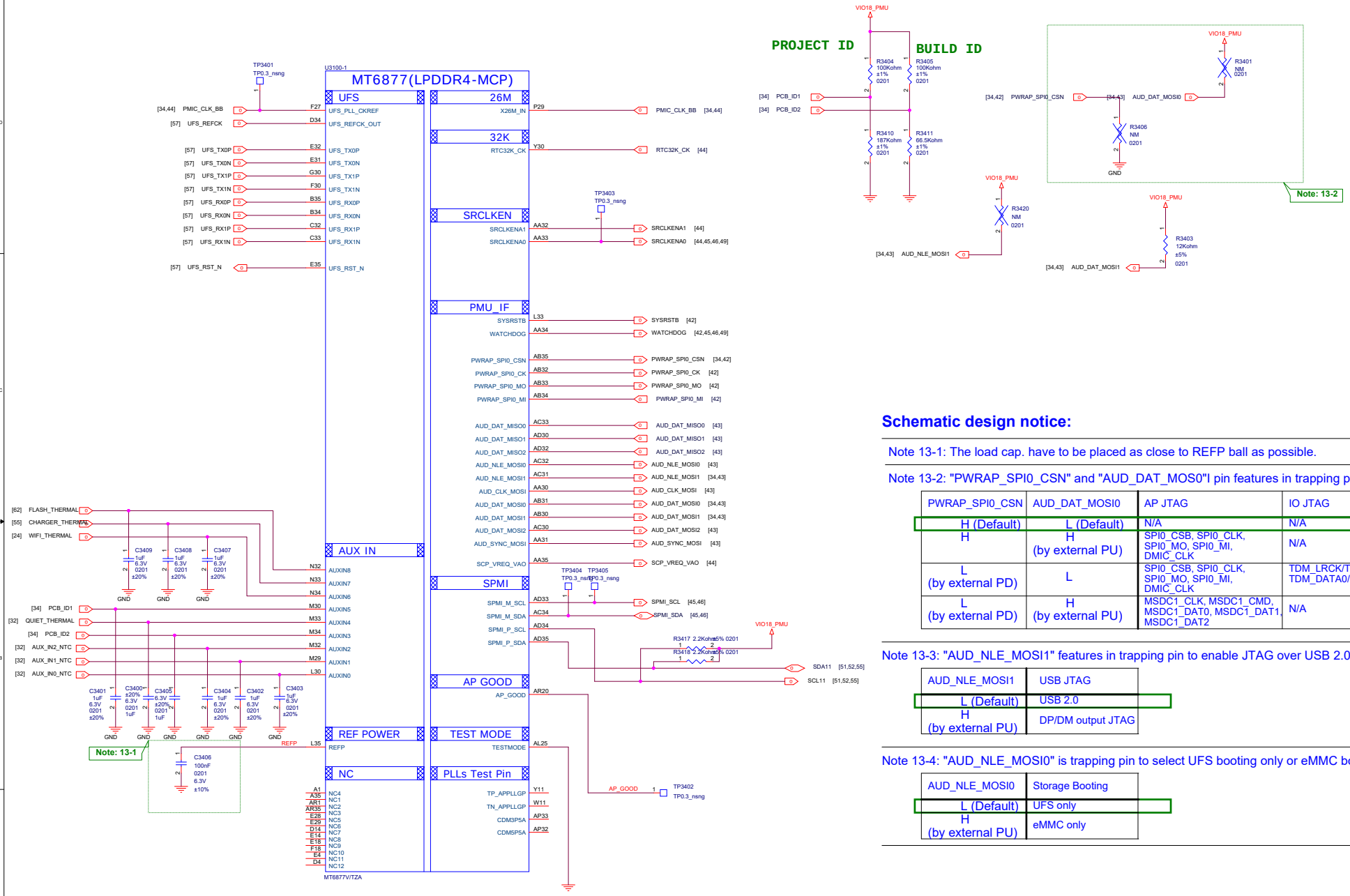
Sheet	



Schematic design notice:

Note 13-1: The load cap. have to be placed as close to REFP ball as possible.

Note 13-2: "PWRAP_SPI0_CSN" and "AUD_DAT_MOS0"I pin features in trapping pin to enable JTAG.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP JTAG	IO JTAG
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	SPI0_CSB, SPI0_CLK, SPI0_MO, SPI0_MI, DMIC_CLK	N/A
L (by external PD)	L	SPI0_CSB, SPI0_CLK, SPI0_MO, SPI0_MI, DMIC_CLK	TDM_LRCK/TDM_BCK/TDM_MCK/ TDM_DATA0/TDM_DATA1
L (by external PD)	H (by external PU)	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	N/A

Note 13-3: "AUD_NLE_MOSI1" features in trapping pin to enable JTAG over USB 2.0 port.

AUD_NLE_MOSI1	USB JTAG
L (Default)	USB 2.0
H (by external PU)	DP/DM output JTAG

Note 13-4: "AUD_NLE_MOSI0" is trapping pin to select UFS booting only or eMMC booting only.

AUD_NLE_MOSI0	Storage Booting
L (Default)	UFS only
H (by external PU)	eMMC only

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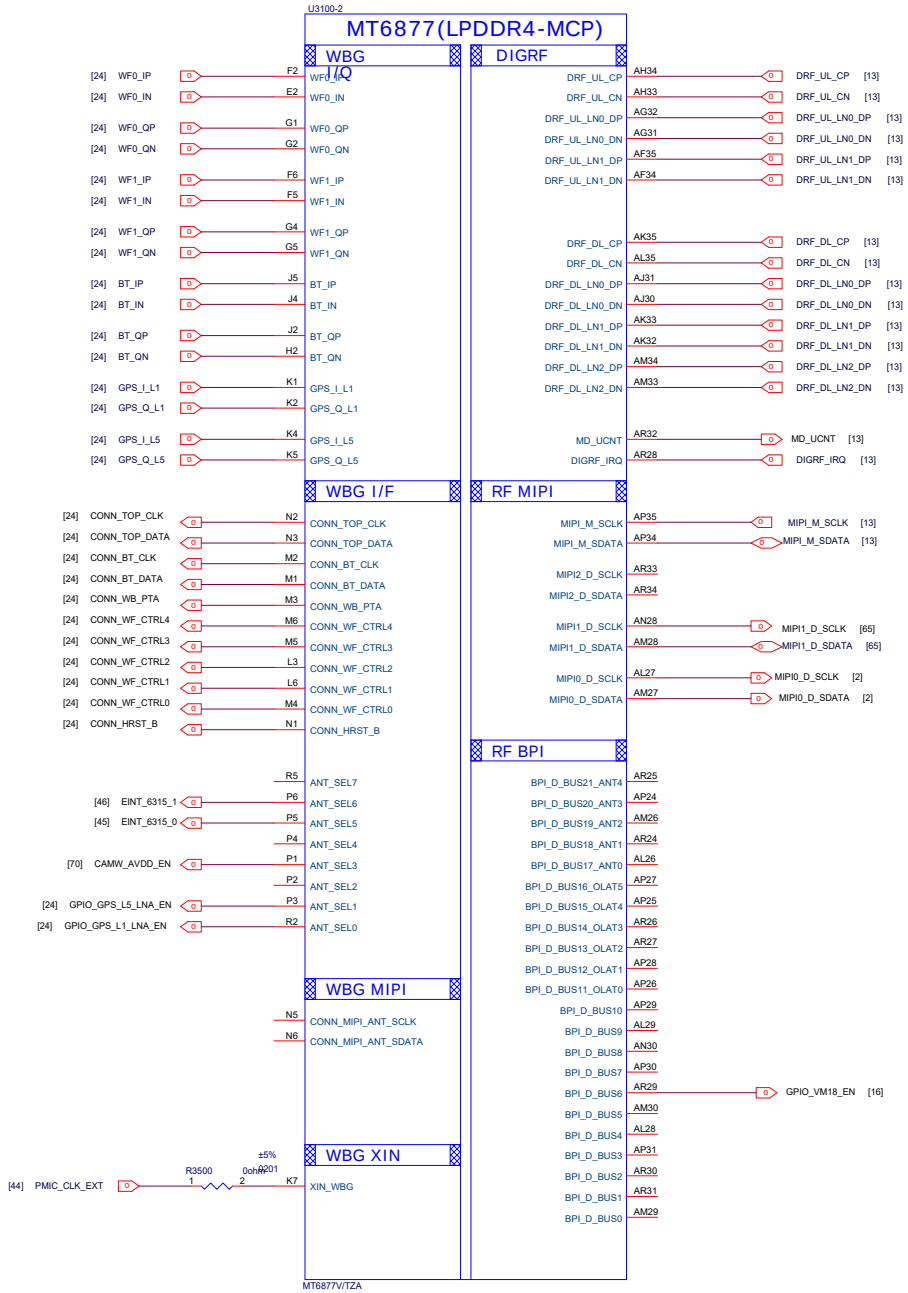

Title	MT6877 RF INTF	
Size C	Document Number MT6877	Rev P0
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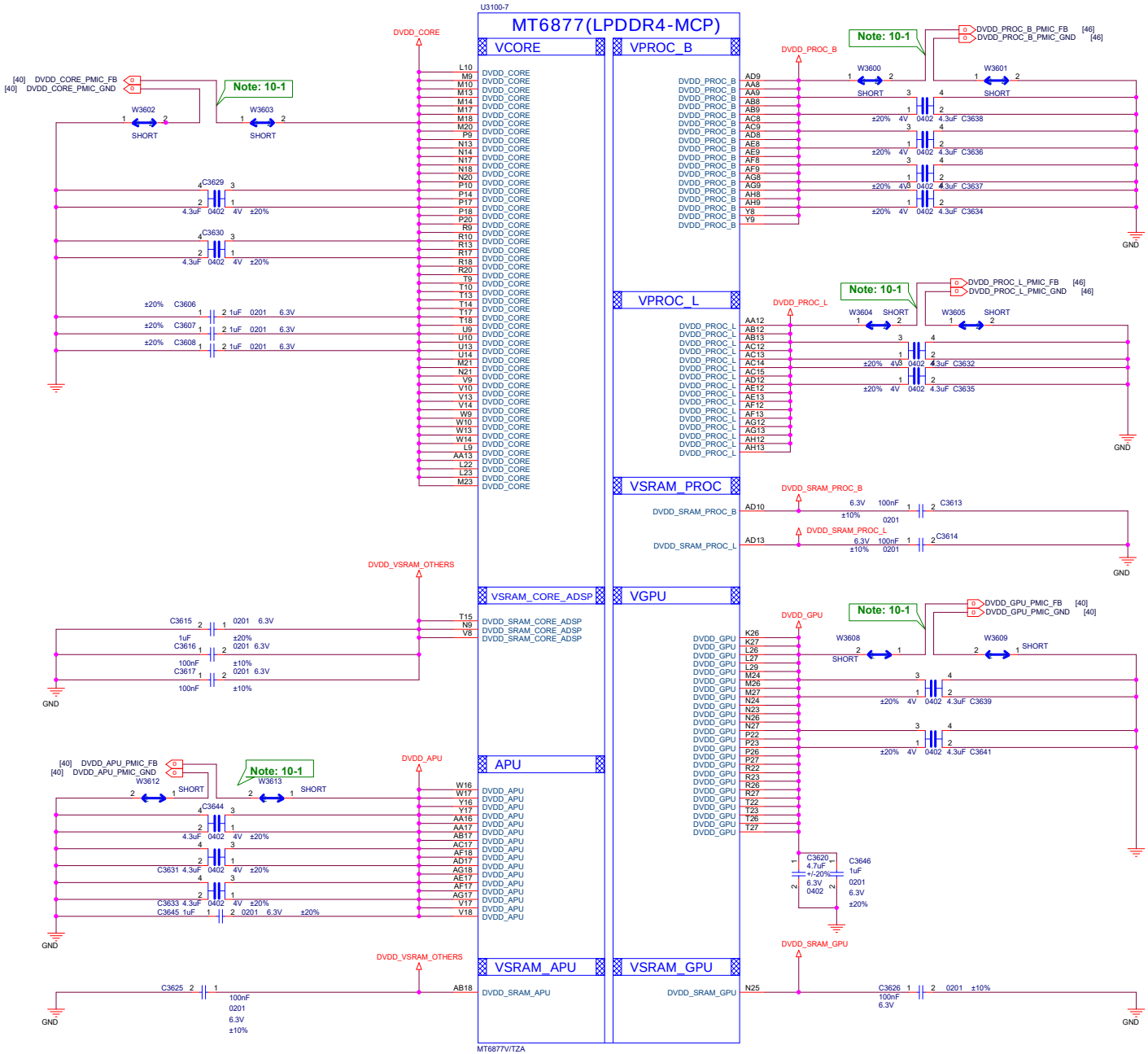

Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1: Differential pair of PMIC remote sense must be close to BB's ball.

Remote sense trace with GND shielding to PMIC (Differential)

Title	MT6873_5GA
Size	C
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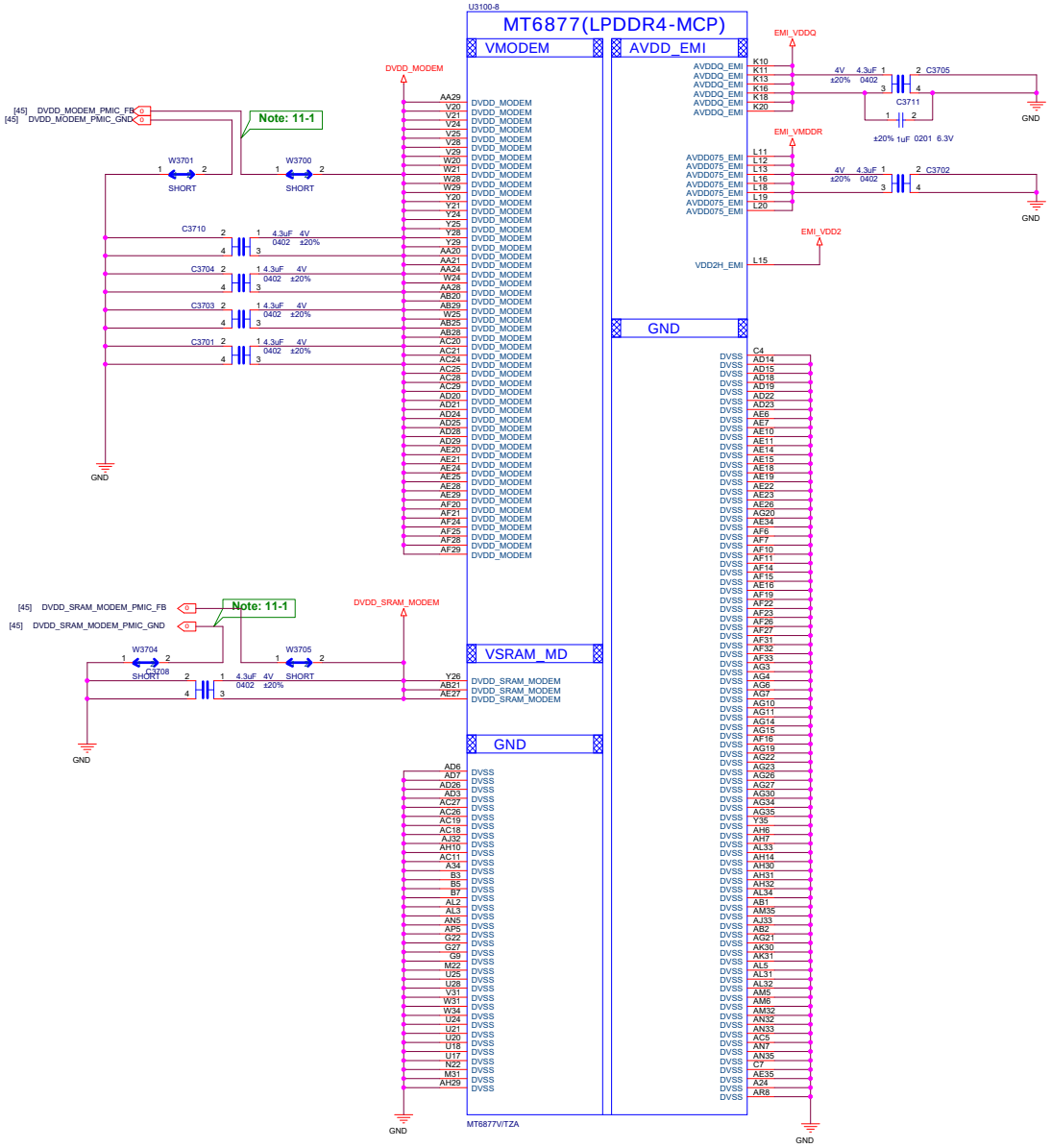

Schematic design notice of "11_BB_POWER_PDN" page.

Note 11-1: Differential pair of PMIC remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Title	MT6873_5GA
Size	A2
Document Number	K16_MAIN
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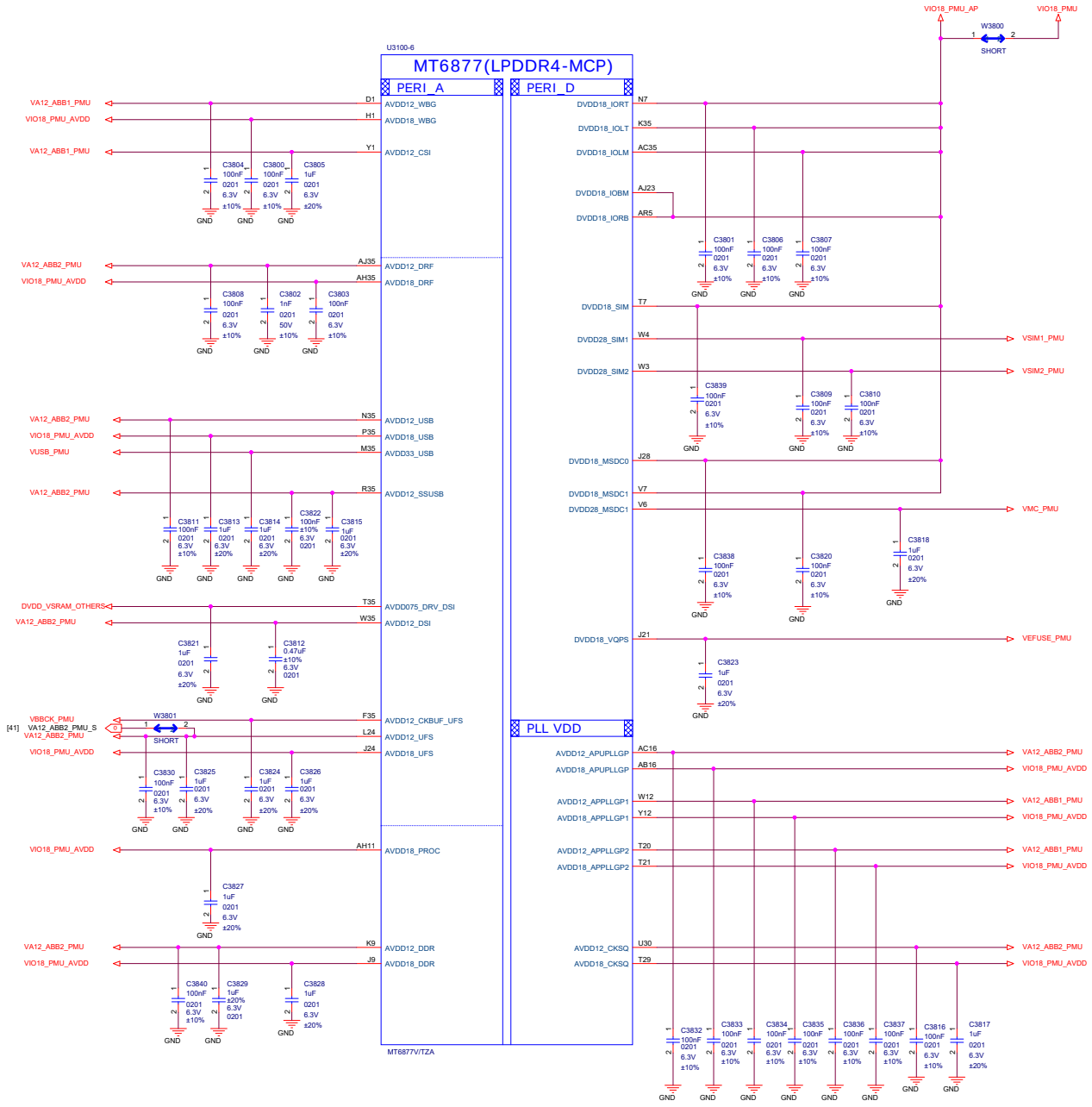

Title	MT6877 PWR3
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U3100-9

MT6877(LPDDR4-MCP)

GND | GND

AC10	DVSS	DVSS	M25
B9	DVSS	DVSS	M28
B10	DVSS	DVSS	N4
B12	DVSS	DVSS	N8
B15	DVSS	DVSS	D7
B17	DVSS	DVSS	D24
B19	DVSS	DVSS	N15
B22	DVSS	DVSS	N16
B26	DVSS	DVSS	N19
B28	DVSS	DVSS	N28
B30	DVSS	DVSS	N29
B32	DVSS	DVSS	AJ1
B33	DVSS	DVSS	P7
C2	DVSS	DVSS	P8
C11	DVSS	DVSS	P11
C14	DVSS	DVSS	P12
C17	DVSS	DVSS	P15
C21	DVSS	DVSS	P16
C26	DVSS	DVSS	P19
C27	DVSS	DVSS	P21
C29	DVSS	DVSS	P24
C31	DVSS	DVSS	P25
C34	DVSS	DVSS	P30
C35	DVSS	DVSS	P31
D2	DVSS	DVSS	P33
D5	DVSS	DVSS	P34
D8	DVSS	DVSS	R7
D12	DVSS	DVSS	R8
D13	DVSS	DVSS	R11
D15	DVSS	DVSS	R15
D16	DVSS	DVSS	R19
D18	DVSS	DVSS	R24
D19	DVSS	DVSS	R25
D20	DVSS	DVSS	R28
D21	DVSS	DVSS	R29
D22	DVSS	DVSS	R32
D25	DVSS	DVSS	D29
D28	DVSS	DVSS	T8
D31	DVSS	DVSS	T11
D32	DVSS	DVSS	T12
D33	DVSS	DVSS	E12
E3	DVSS	DVSS	T16
E5	DVSS	DVSS	T19
E6	DVSS	DVSS	T24
E8	DVSS	DVSS	T25
E10	DVSS	DVSS	T30
E15	DVSS	DVSS	T31
E17	DVSS	DVSS	T33
E21	DVSS	DVSS	T34
E23	DVSS	DVSS	U6
E26	DVSS	DVSS	U8
E30	DVSS	DVSS	U11
E33	DVSS	DVSS	U12
E34	DVSS	DVSS	U15
AG24	DVSS	DVSS	U16
F4	DVSS	DVSS	U19
F7	DVSS	DVSS	U7
F8	DVSS	DVSS	U23
F10	DVSS	DVSS	U26
F12	DVSS	DVSS	AC7
F15	DVSS	DVSS	U31
F16	DVSS	DVSS	V11
F19	DVSS	DVSS	V12
F21	DVSS	DVSS	V15
F23	DVSS	DVSS	V16
F25	DVSS	DVSS	V19
F28	DVSS	DVSS	V22
F29	DVSS	DVSS	V23
F31	DVSS	DVSS	V26
F32	DVSS	DVSS	V27
F33	DVSS	DVSS	W7
F34	DVSS	DVSS	W15
G3	DVSS	DVSS	W18
G28	DVSS	DVSS	W19
G31	DVSS	DVSS	W22
H3	DVSS	DVSS	W23
H5	DVSS	DVSS	W26
H20	DVSS	DVSS	W27
H21	DVSS	DVSS	W30
H22	DVSS	DVSS	AJ2
H30	DVSS	DVSS	Y2
H31	DVSS	DVSS	Y3
J11	DVSS	DVSS	Y4
J12	DVSS	DVSS	Y7
J13	DVSS	DVSS	Y10
J14	DVSS	DVSS	Y14
J16	DVSS	DVSS	Y15
J19	DVSS	DVSS	Y18
J20	DVSS	DVSS	Y19
AG16	DVSS	DVSS	Y22
K29	DVSS	DVSS	Y23
K3	DVSS	DVSS	Y31
K6	DVSS	DVSS	AJ7
K12	DVSS	DVSS	AA5
AC6	DVSS	DVSS	AA6
K14	DVSS	DVSS	AA7
C10	DVSS	DVSS	AA10
K17	DVSS	DVSS	AA11
K19	DVSS	DVSS	AA14
K21	DVSS	DVSS	AA15
AN34	DVSS	DVSS	AA18
K24	DVSS	DVSS	AA19
K25	DVSS	DVSS	AA22
K28	DVSS	DVSS	AA23
L1	DVSS	DVSS	AA26
L2	DVSS	DVSS	AA27
L5	DVSS	DVSS	AJ8
L7	DVSS	DVSS	AB6
L8	DVSS	DVSS	H6
L21	DVSS	DVSS	AB10
L25	DVSS	DVSS	AB11
L28	DVSS	DVSS	AB14
AF3	DVSS	DVSS	AB15
M7	DVSS	DVSS	AB19
M8	DVSS	DVSS	AB22
M11	DVSS	DVSS	AB23
M12	DVSS	DVSS	AB26
M15	DVSS	DVSS	AB27
M16	DVSS	DVSS	AK5
M19	DVSS	DVSS	W8
AG25	DVSS	DVSS	Y27
AG28	DVSS	DVSS	AD27
E19	DVSS	DVSS	AM2
E27	DVSS	DVSS	AN2
F14	DVSS	DVSS	AR3
F24	DVSS	DVSS	AR4
R12	DVSS	DVSS	J8
R16	DVSS	DVSS	K8
R21	DVSS	DVSS	AD11
U7	DVSS	DVSS	E1
H8	DVSS	DVSS	G11
J6	DVSS	DVSS	G13
AG29	DVSS	DVSS	G18
AJ29	DVSS	DVSS	G20
AK34	DVSS	DVSS	AK29
	DVSS	DVSS	

MT6877V/TZA

GND GND

Title	MT6877 GND	
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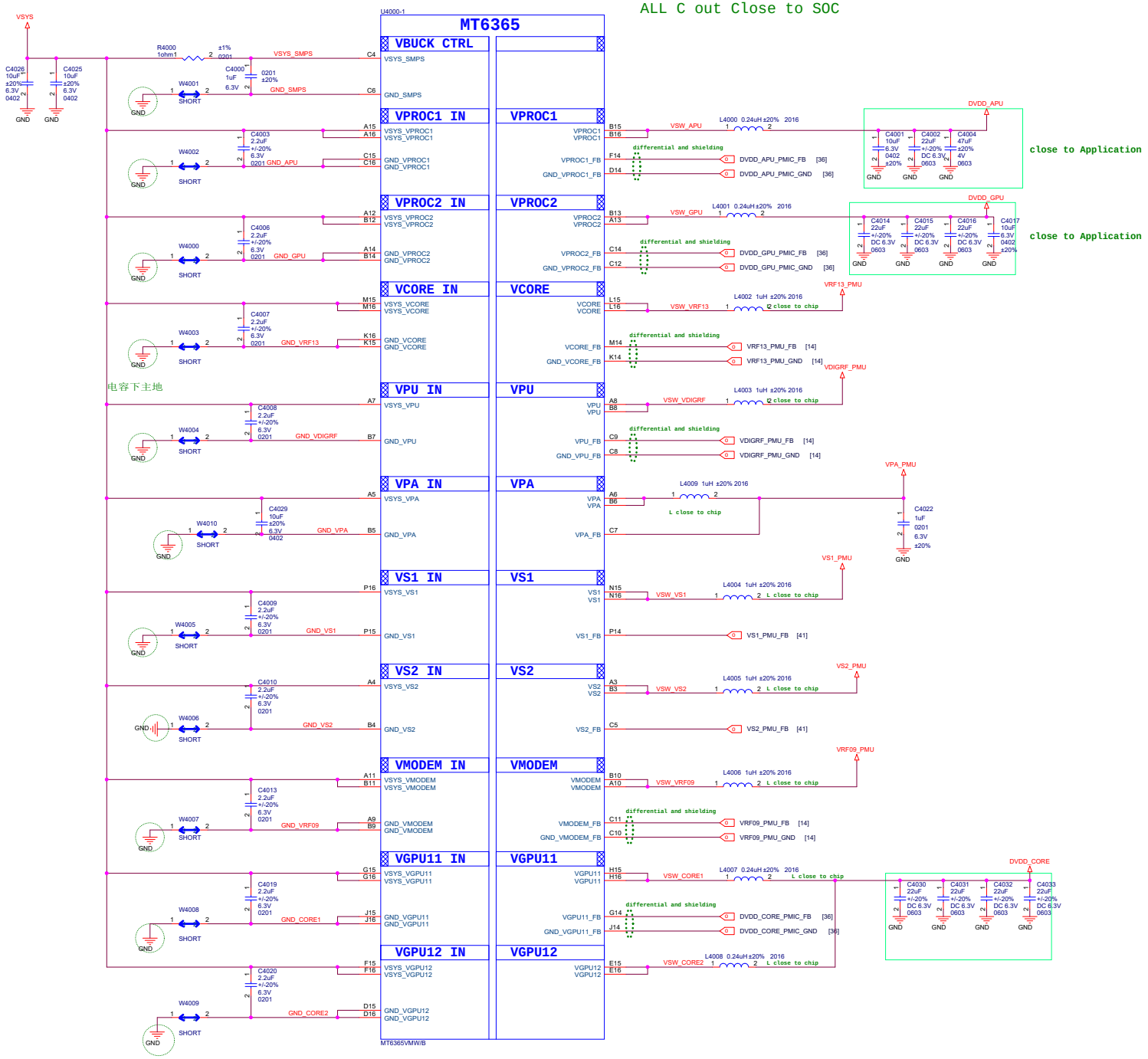
ALL C out Close to SOC



Title	MT6365 BUCK	
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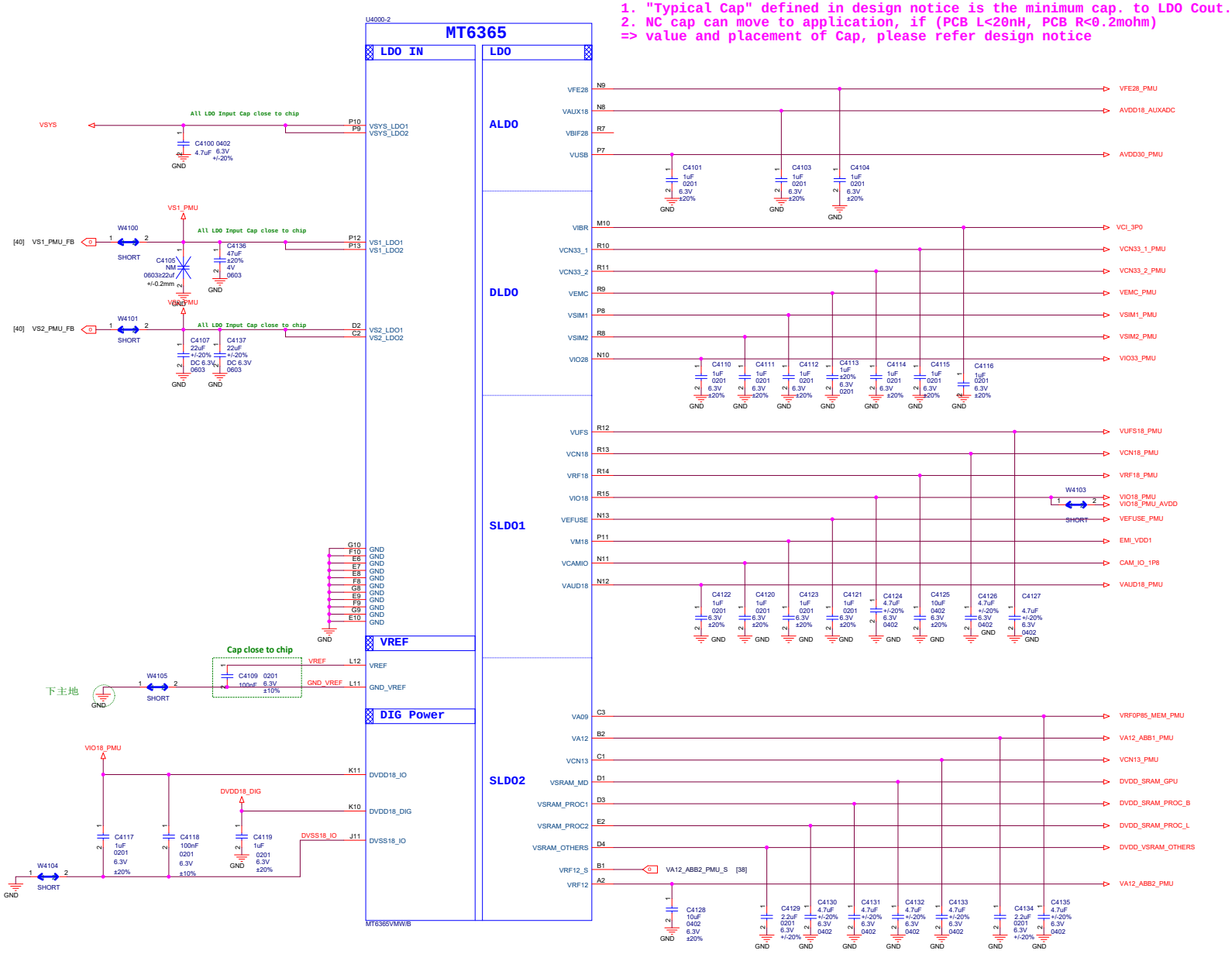
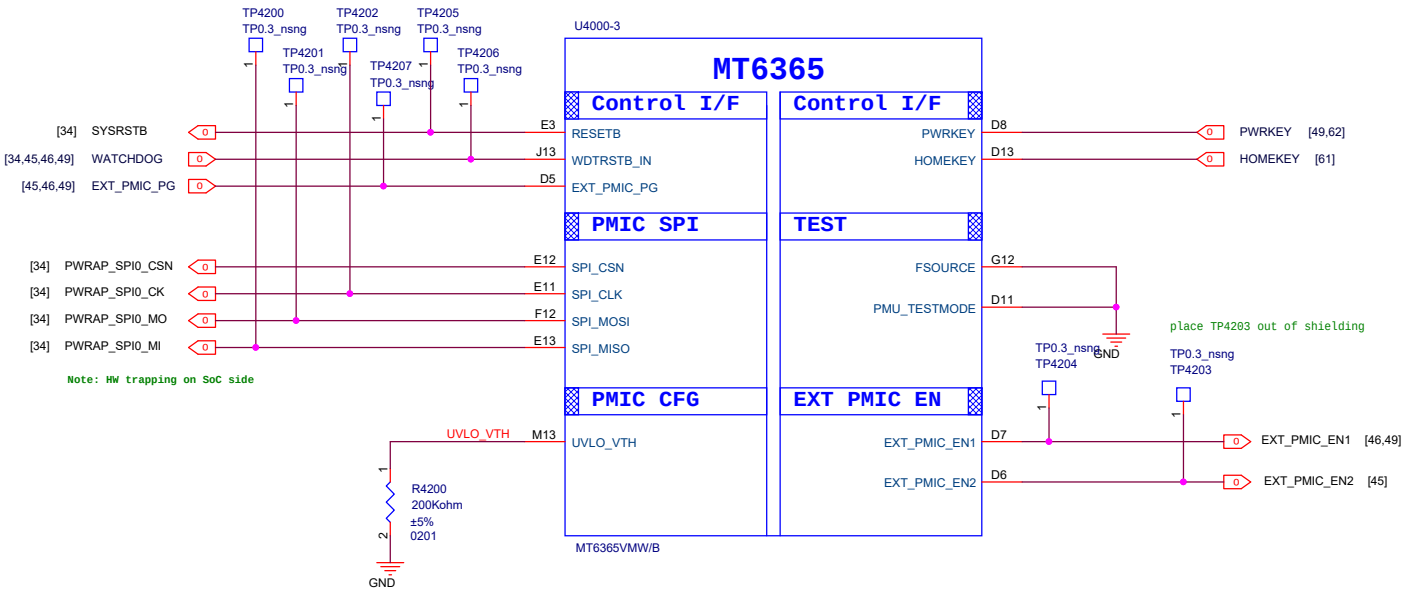
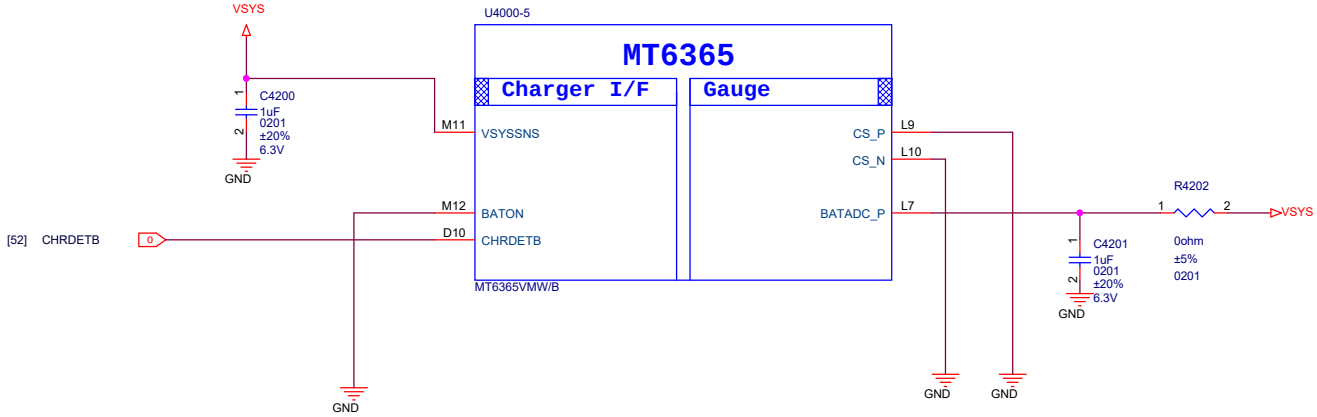
1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2mohm)
=> value and placement of Cap, please refer design notice

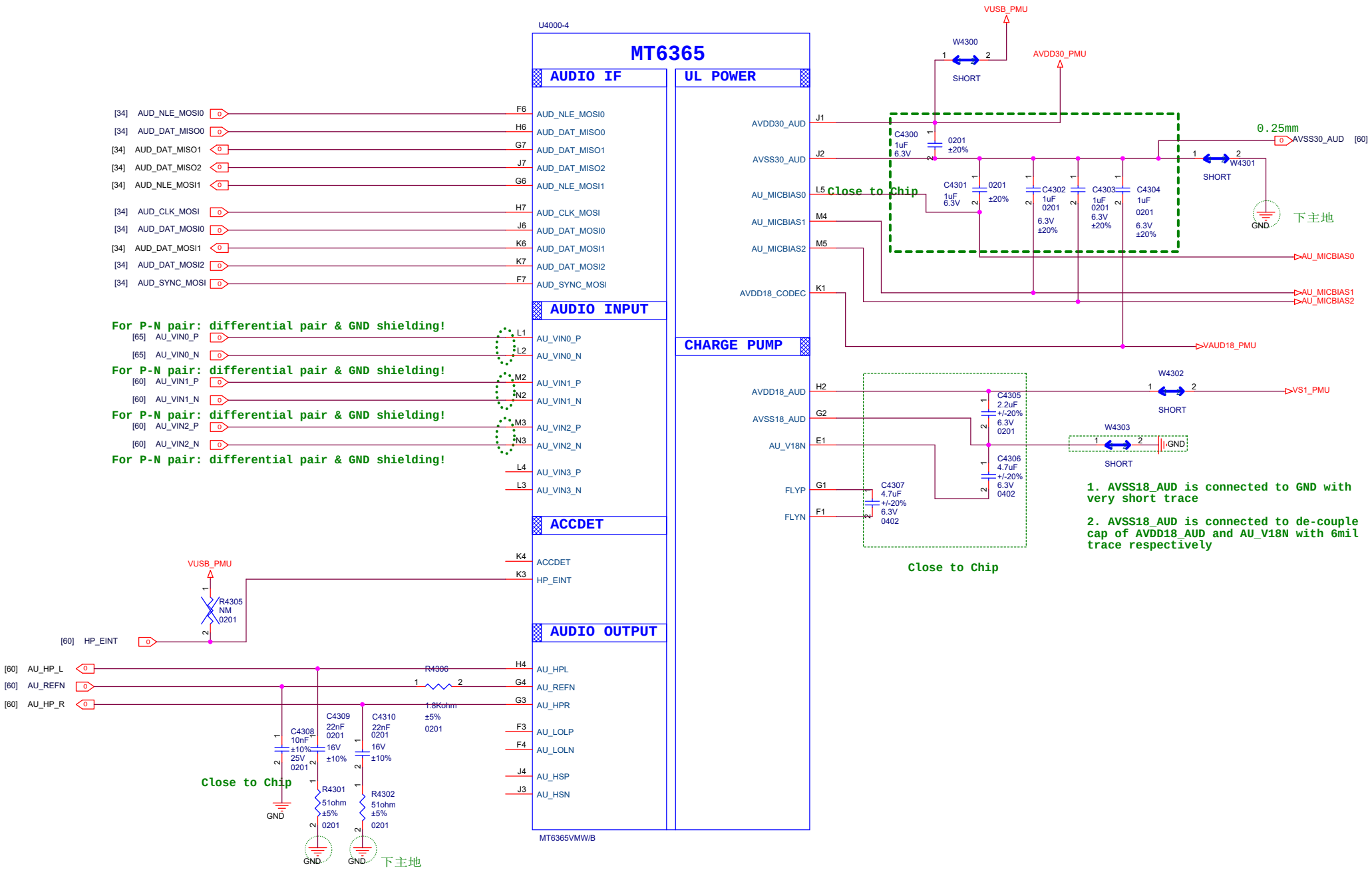


Title	MT6365 LDO	
Size A2	Document Number MT6877	Rev P0
Date: Thursday, August 26, 2021	Sheet	





Title	MT6365 General	
Size A3	Document Number MT6877	Rev P0
Date: Thursday, August 26, 2021	Sheet	



-AU_HPL and AU_HPR should be routed as single end signal and be guarded by GND, up and down, left and right respectively

-The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN is " GND AU_HPL AU_REFN AU_HPR GND"

Title	MT6365 AUDIO	
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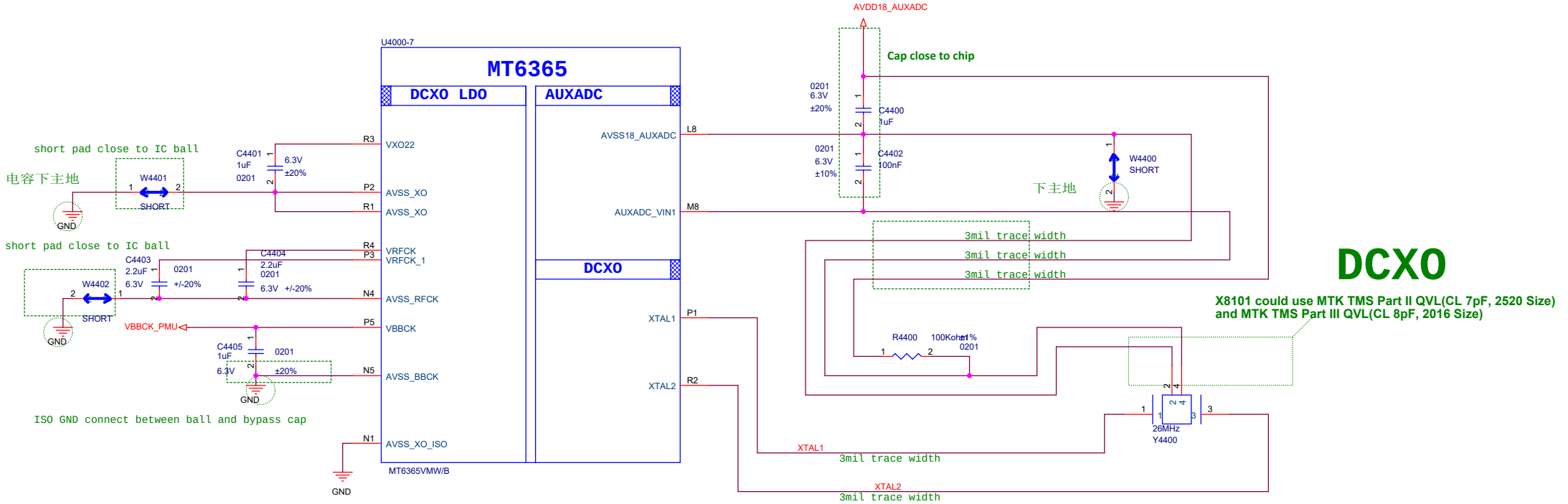

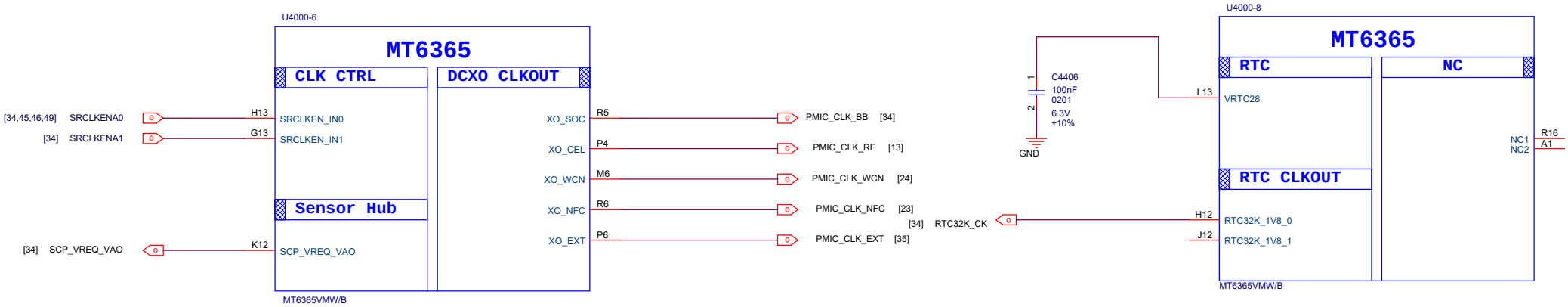

Title	MT6365 CLOCK	
Size A3	Document Number MT6877	Rev P0
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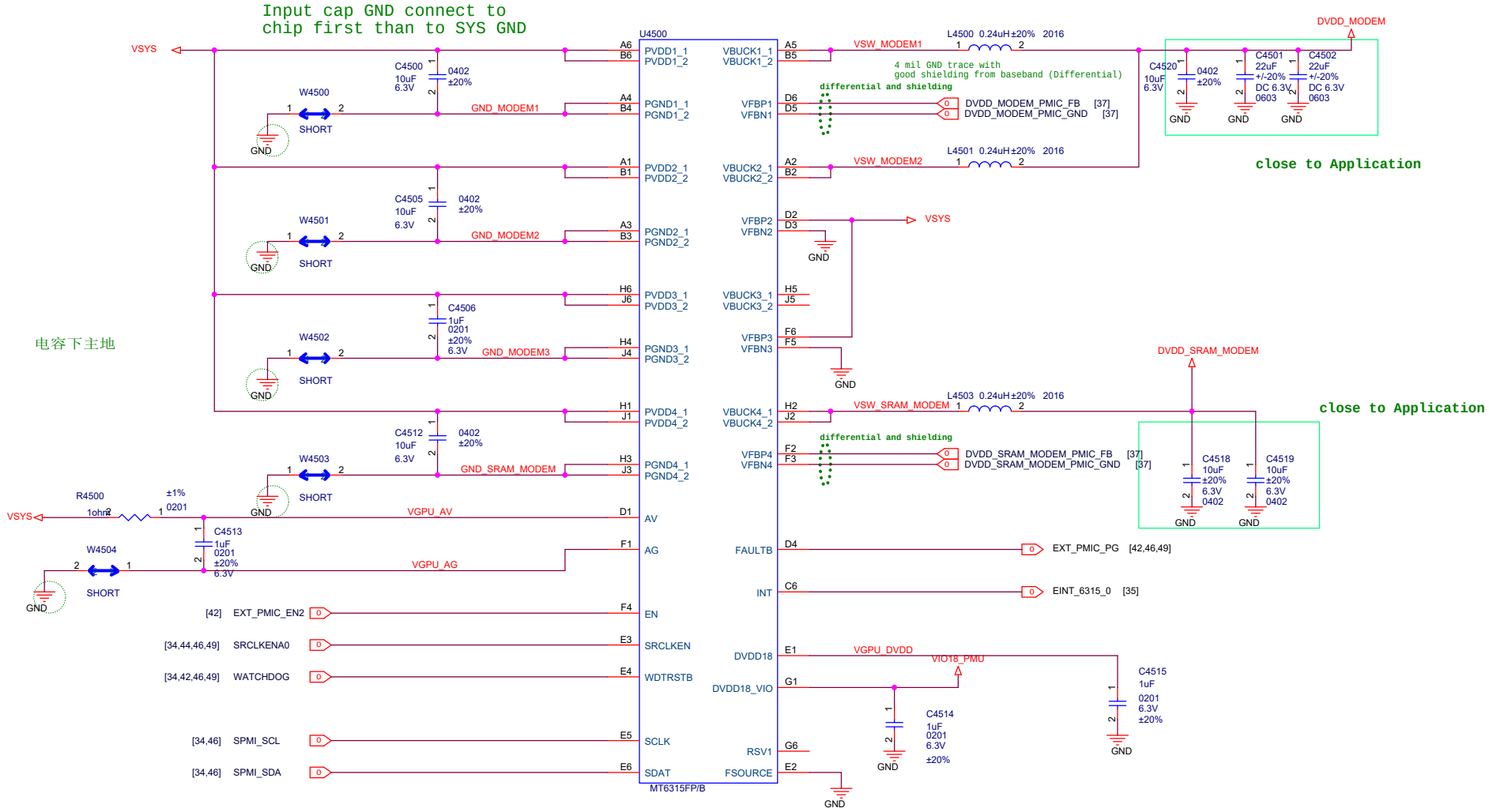
MT6315 4-Phase Buck (GPU)



Title	MT6315 VMD	
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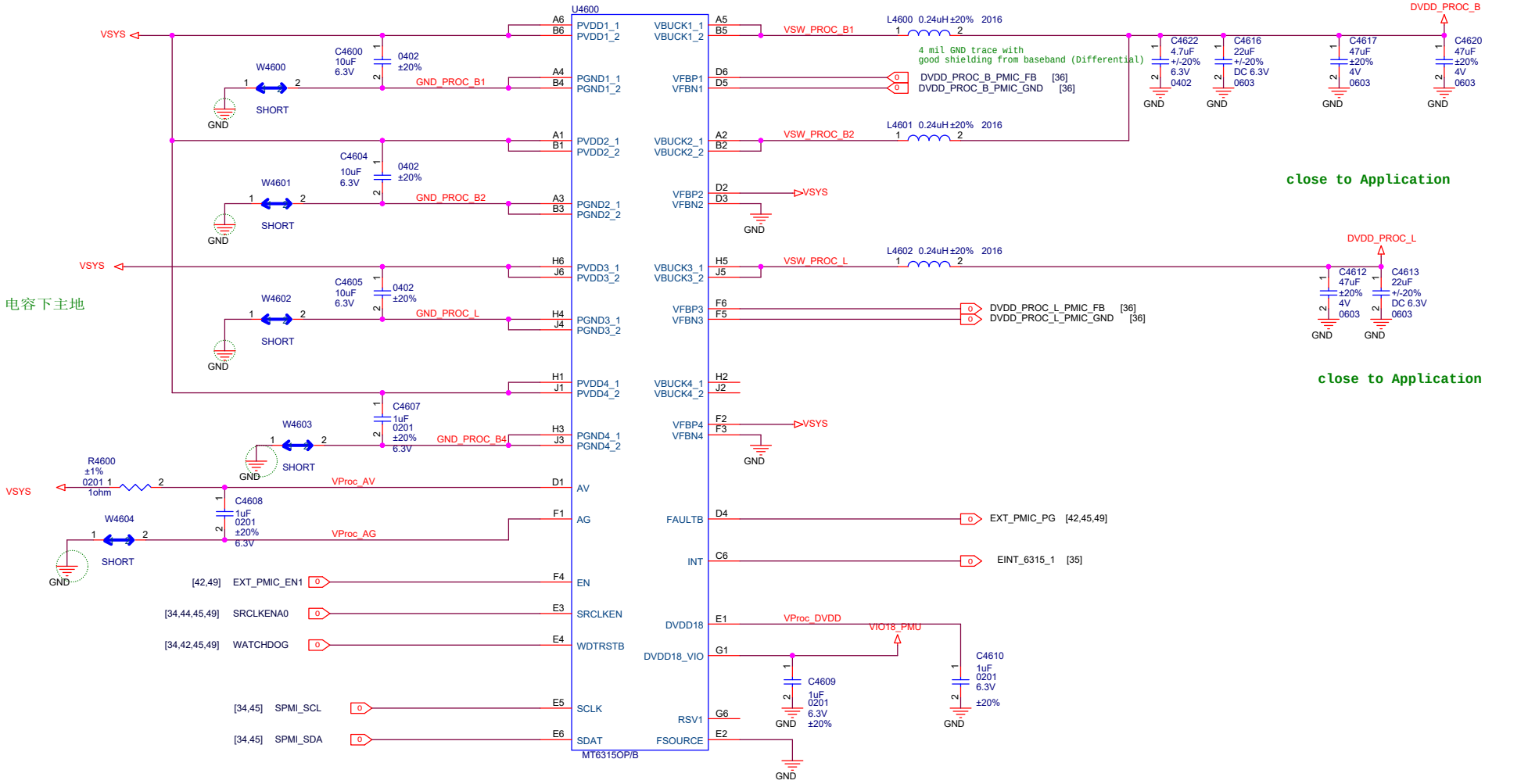
MT6315 4-Phase Buck (CPU)

Input cap GND connect to
chip first than to SYS GND

ALL C out Close to SOC



Title	MT6315 Vproc	
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Title	MT6315 Reserved	
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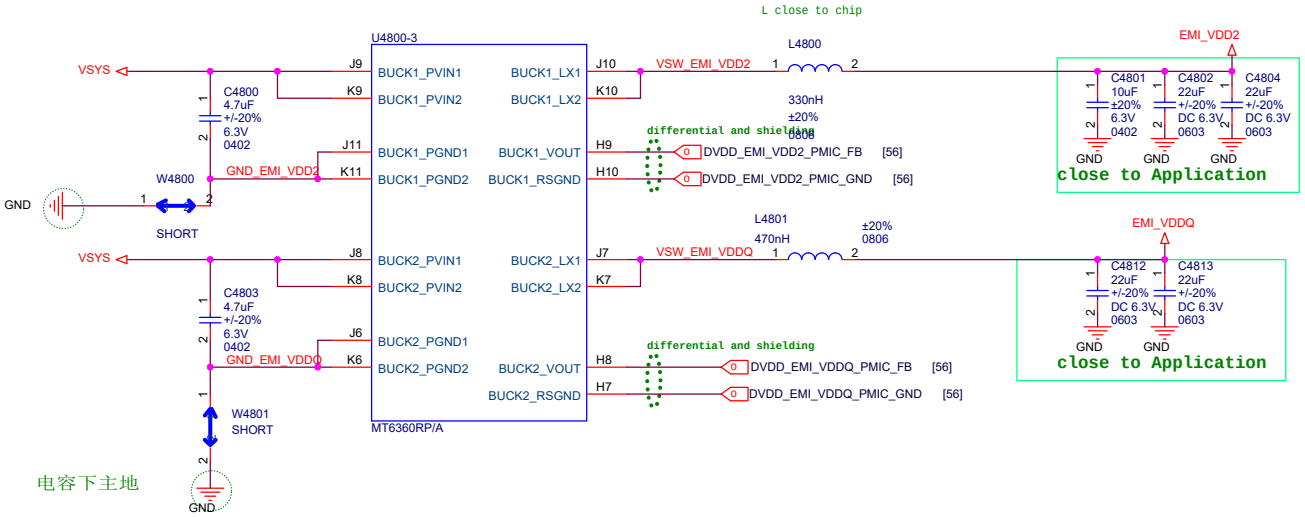
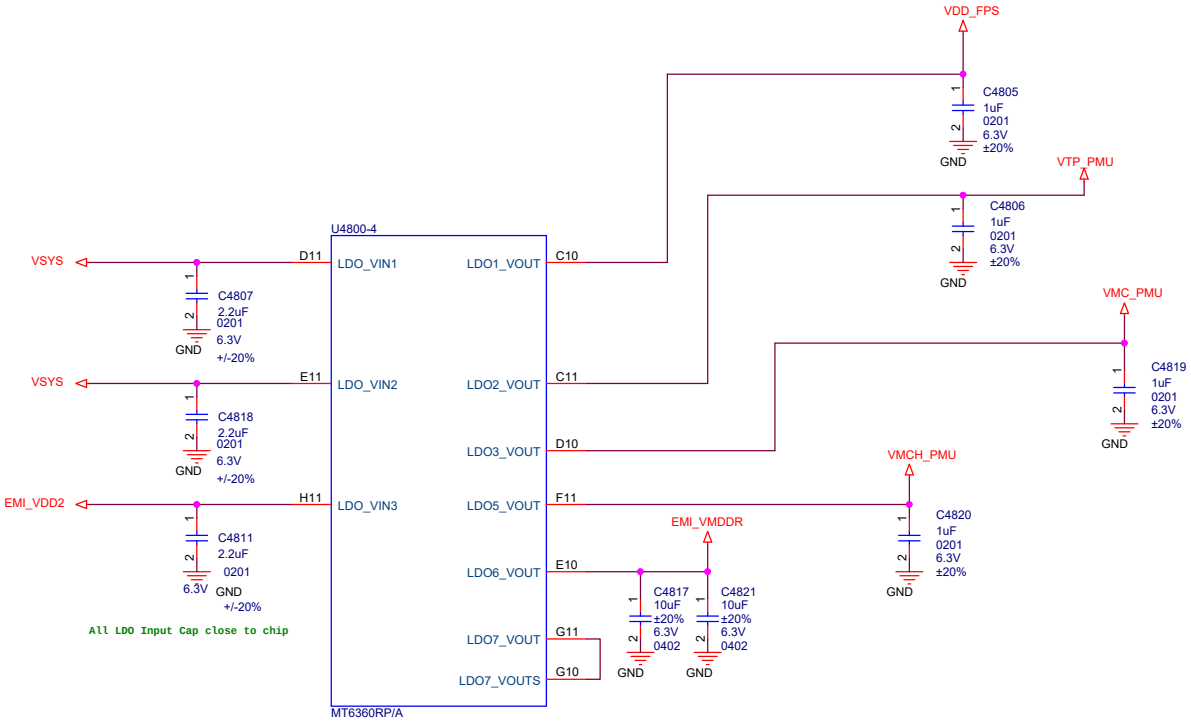
ALL C out Close to DDR





LDO1	VFP
LDO2	VTP
LDO3	VMC
LDO5	SD_CARD_2P95
LDO6	
LDO7	VMDDR_EN

Title	MT6360 BUCK LDO	
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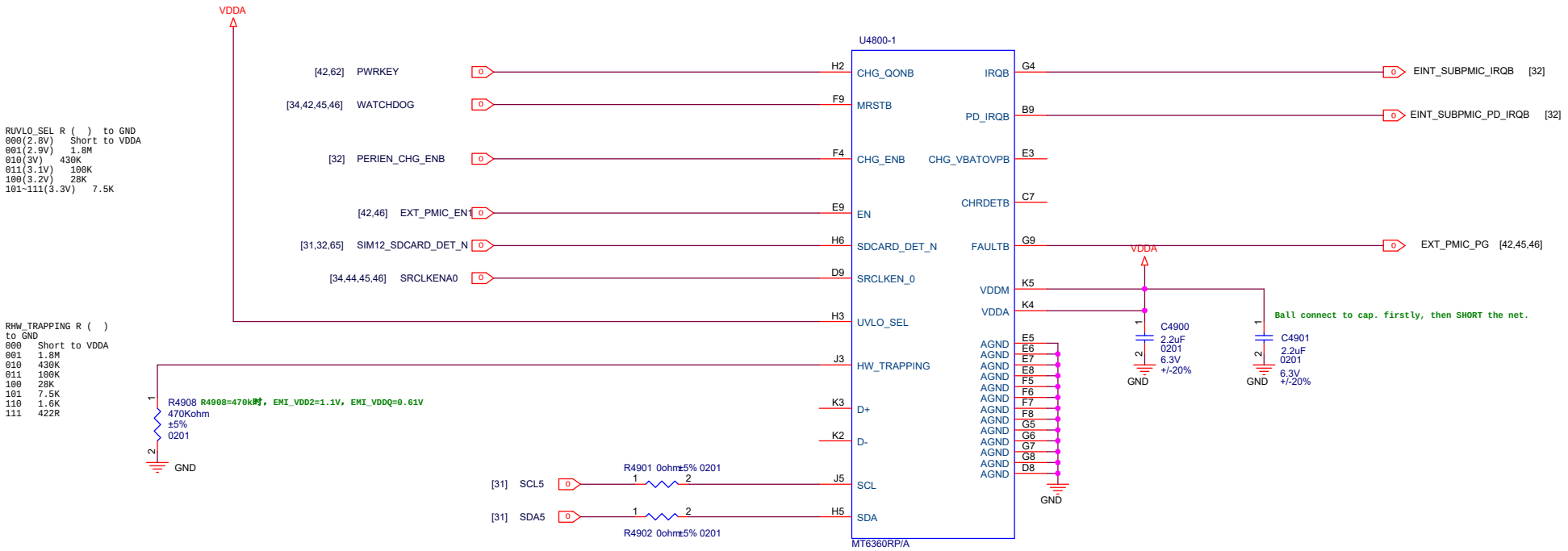
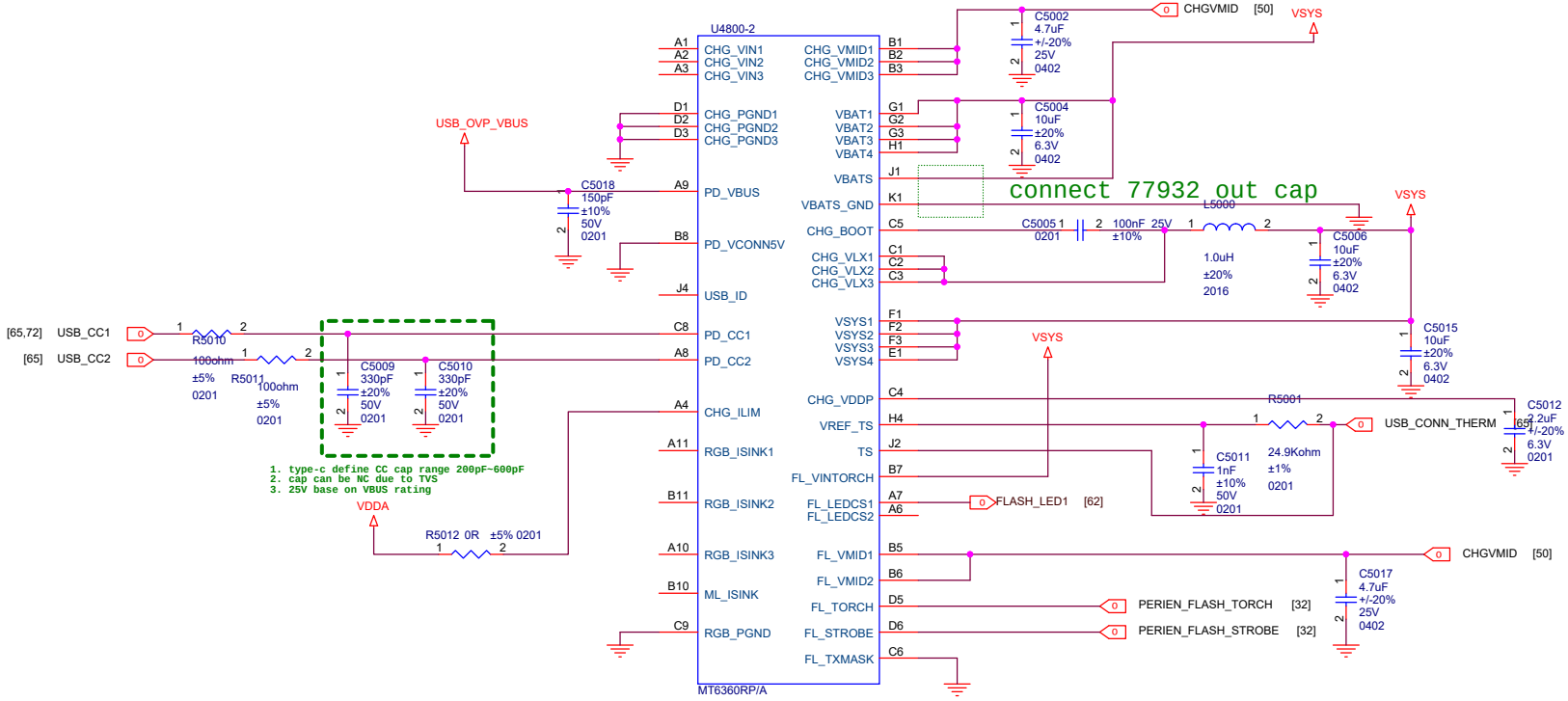


Refer to MT6360 Application Note
If SDA trace distance > 1001 mil,
adding a Rs on this trace is suggested.

Title	MT6360 General	
Size A3	Document Number MT6877	Rev P0
Date: Thursday, August 26, 2021	Sheet	



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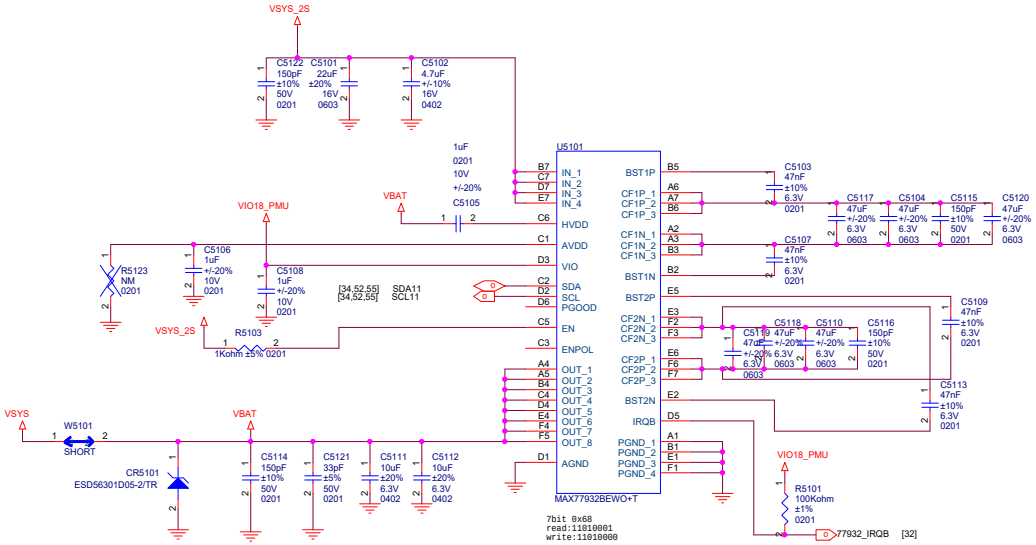
Size A3	Document Number MT6877	Rev P0
Date: Thursday, August 26, 2021	Sheet	



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MI PHONE		
Title	MT6873_5GA	
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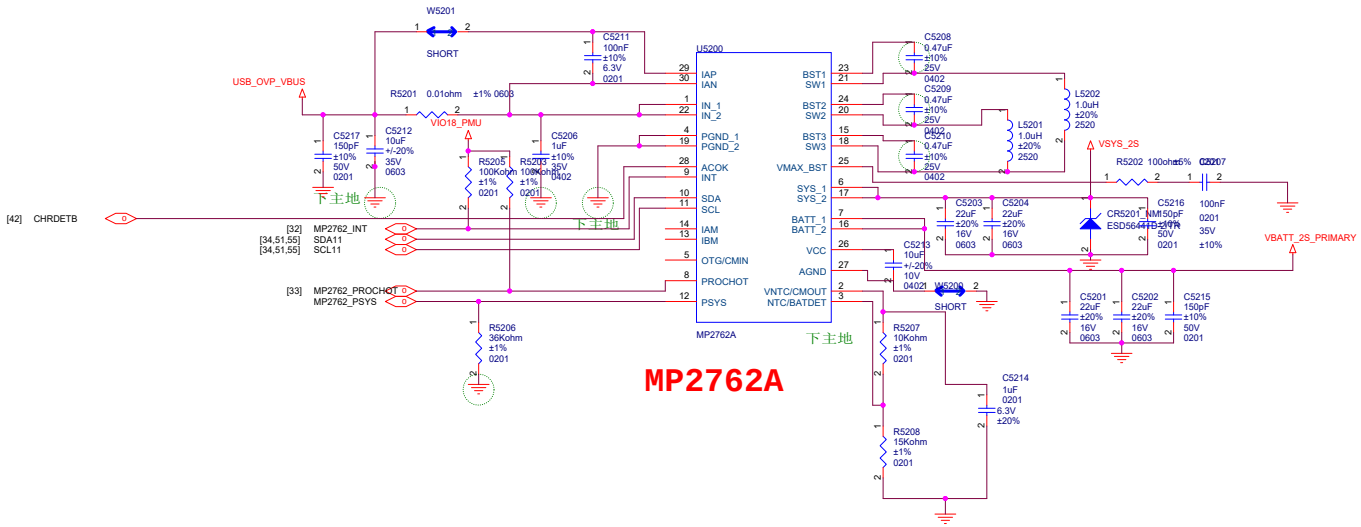

MI PHONE		
Title	MT6873_5GA	
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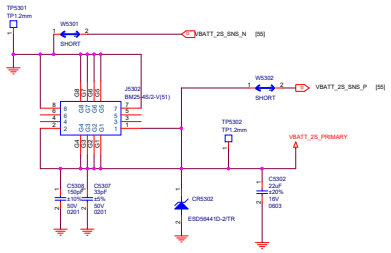
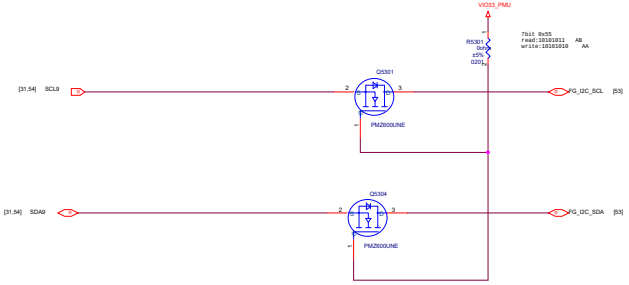
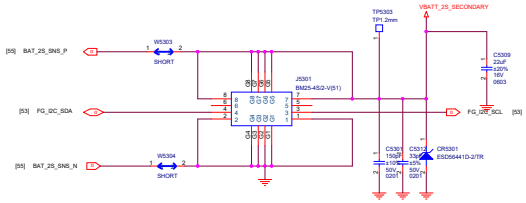
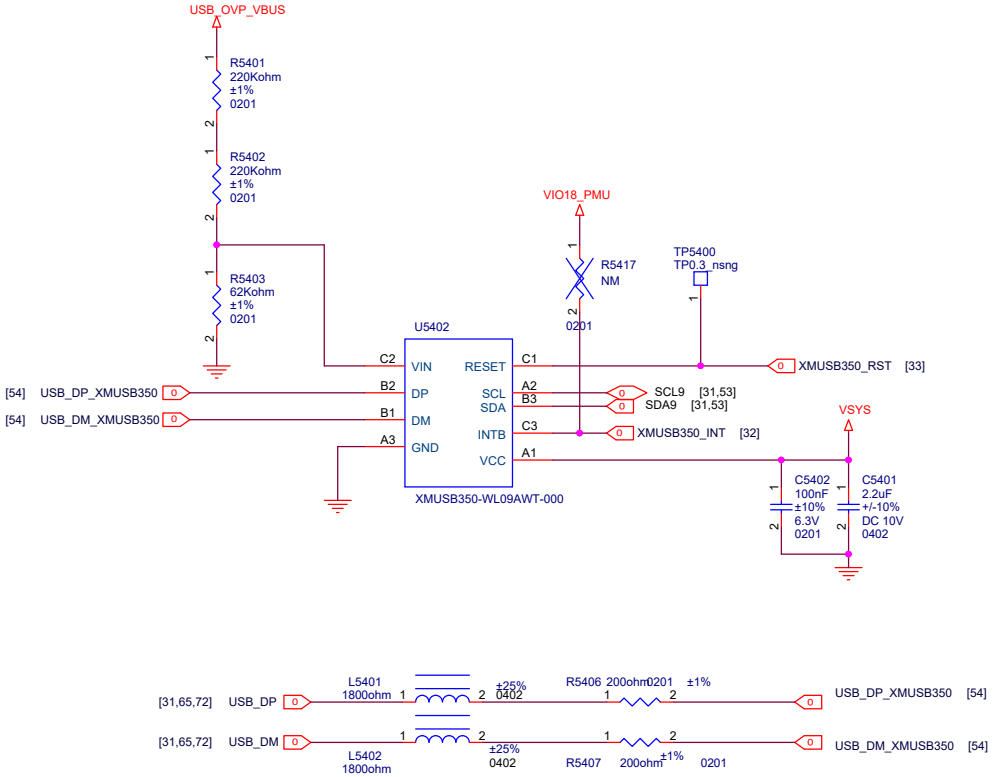
PRIMARY BAT CON





SECONDARY BAT CON





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Title		
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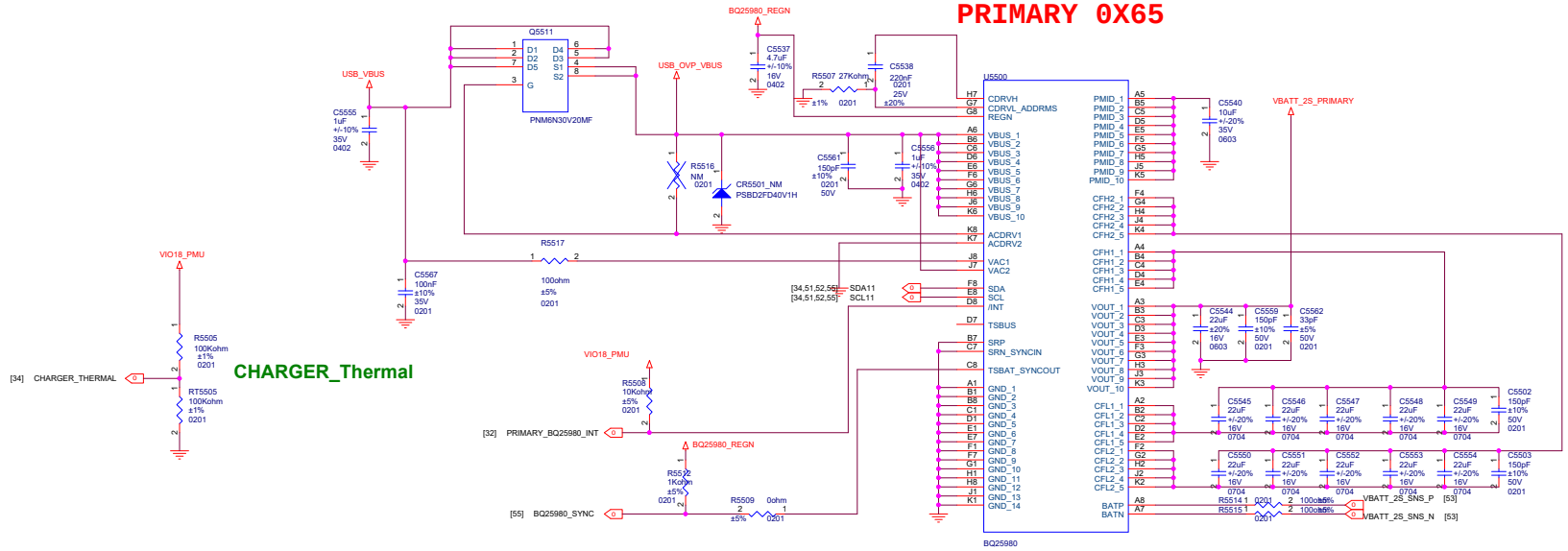
PRIMARY 0X65



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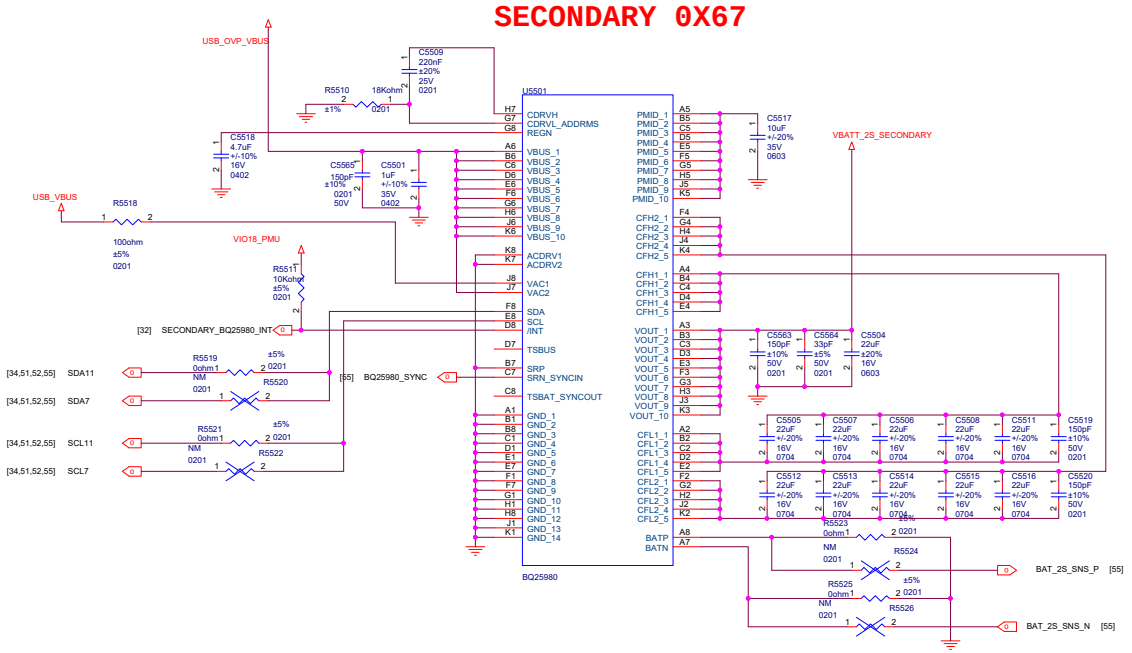

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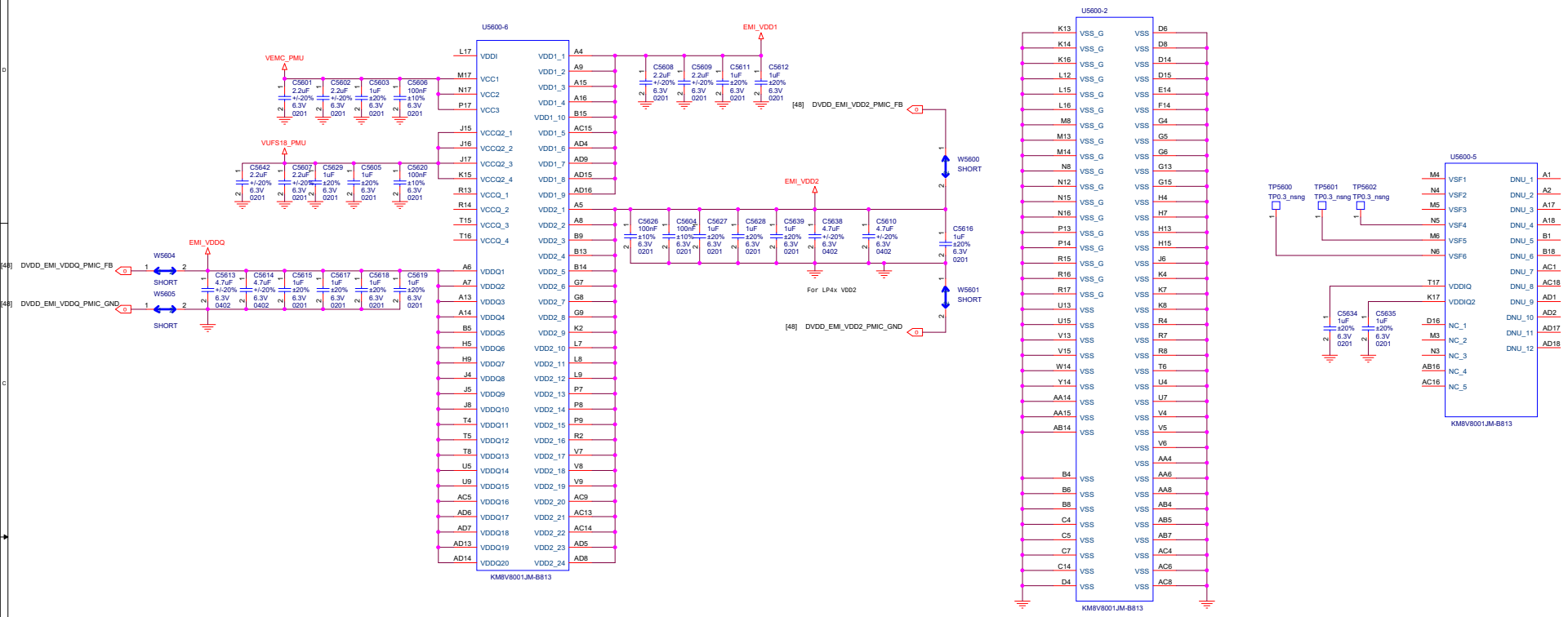

Title	K16_MAIN
Size A2	Document Number MEMORY POWER
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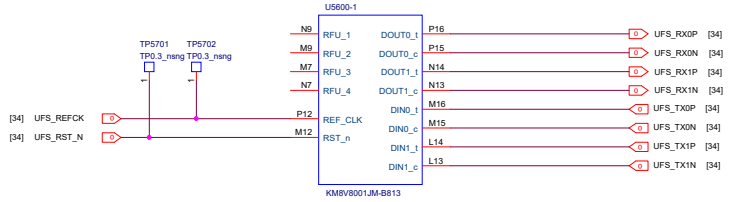
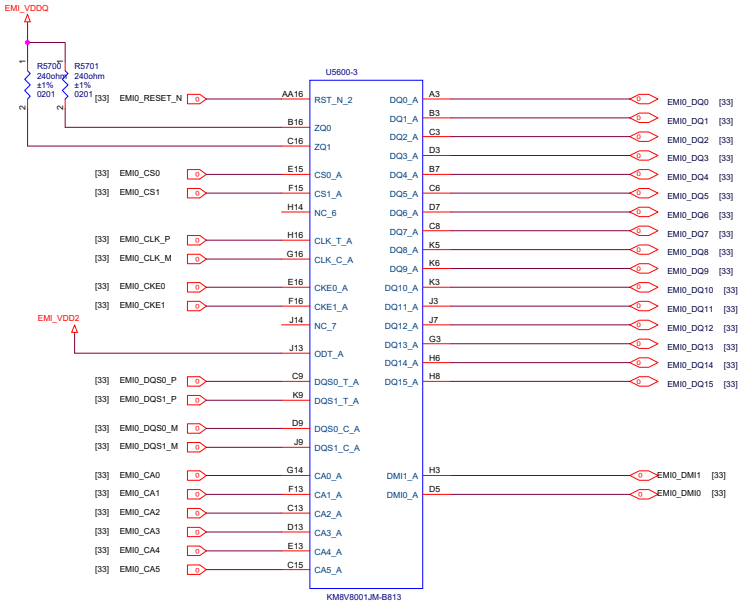
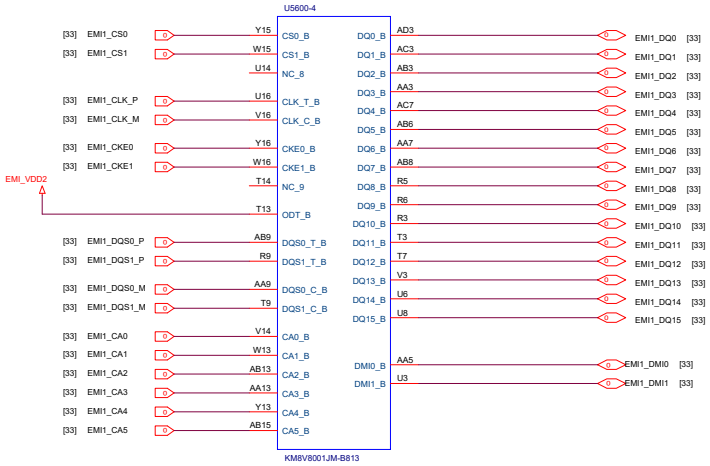
UFS 2.2



LPDDR4/4x





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Size A2	Document Number MEMORY UFS/LPDDR4X	Rev P0
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MI PHONE		
Title K16_MAIN		
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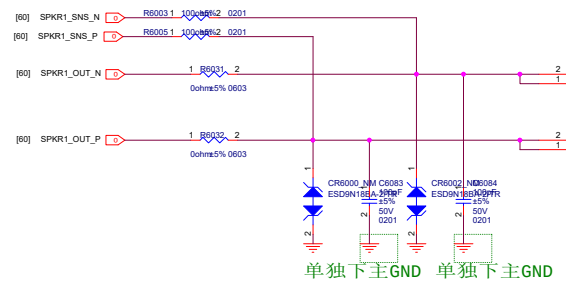
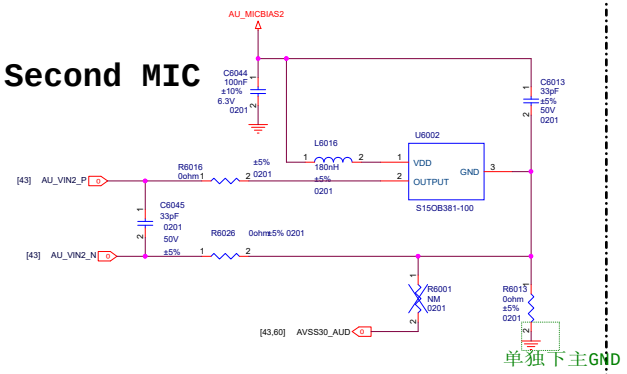
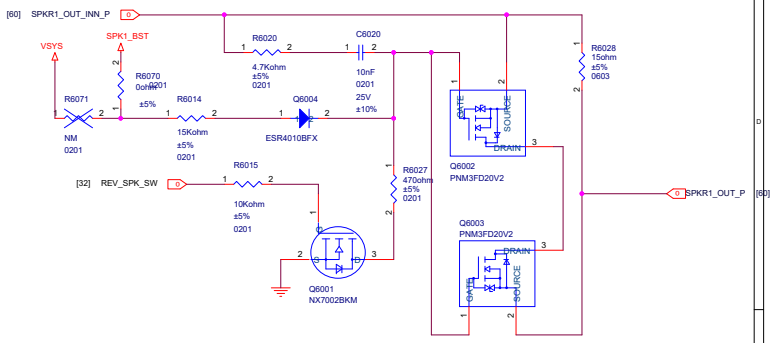
SPK

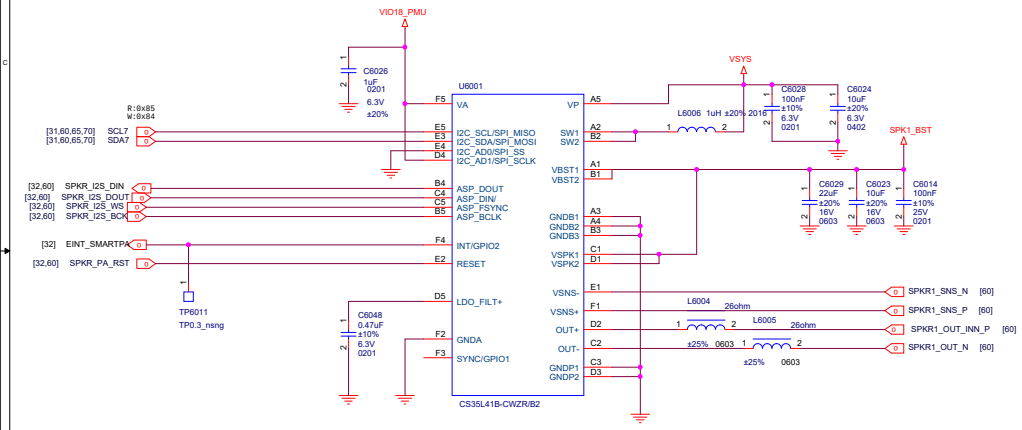


Second MIC





SPKR PA



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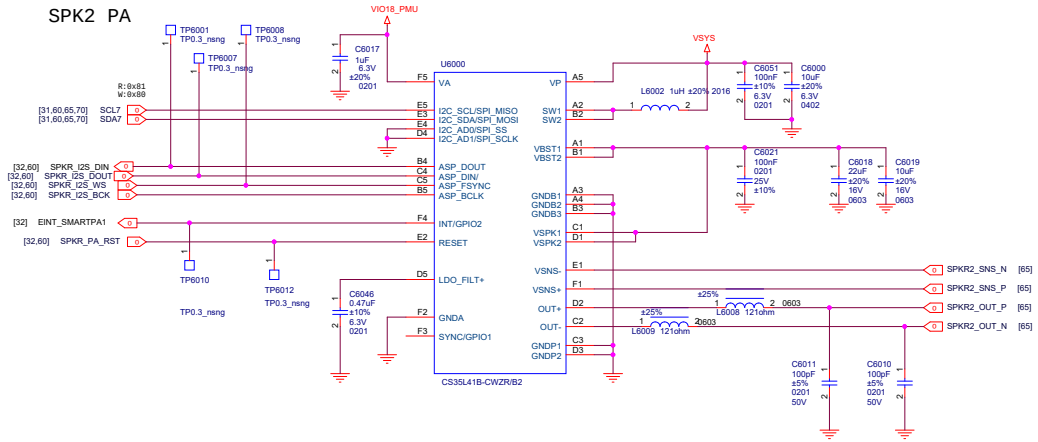

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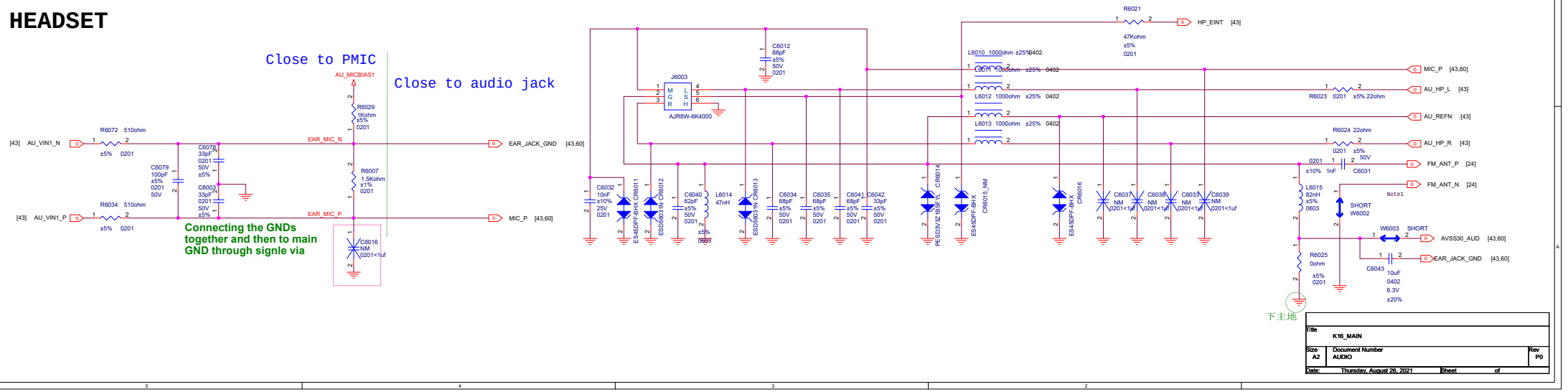

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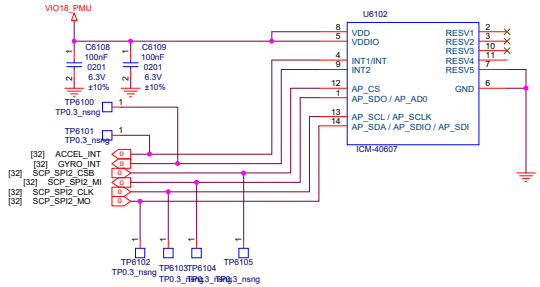
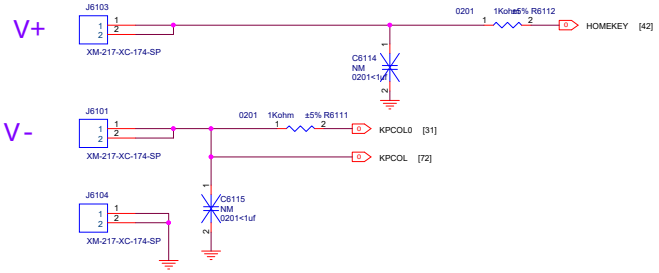
A+G1



HAPTICS

Sidekey

音量键PCB 上要加丝印



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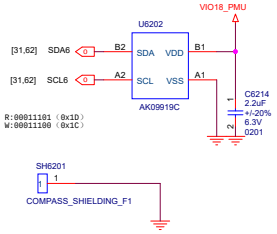
COMPASS



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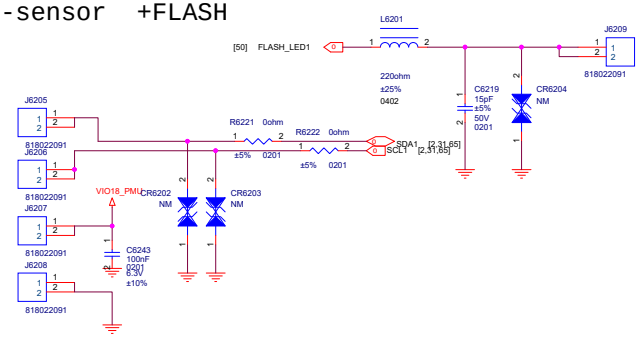

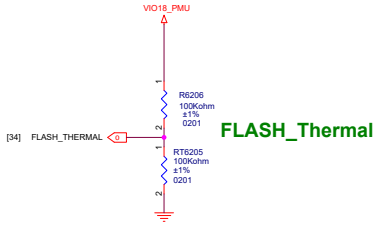

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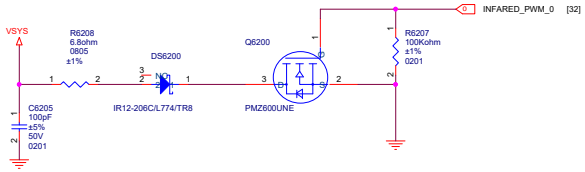

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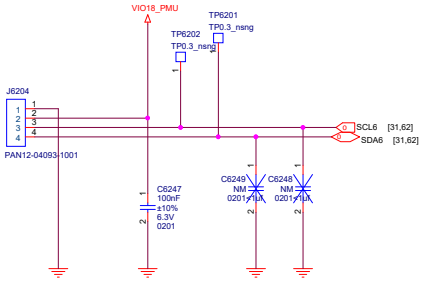
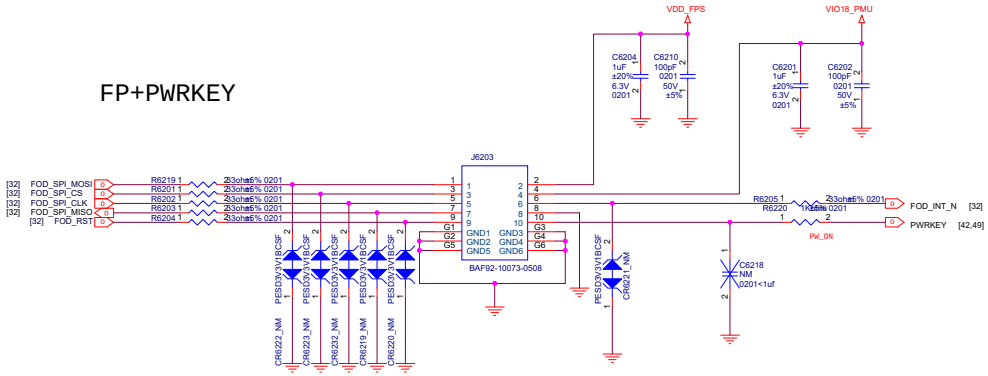


FP+PWRKEY



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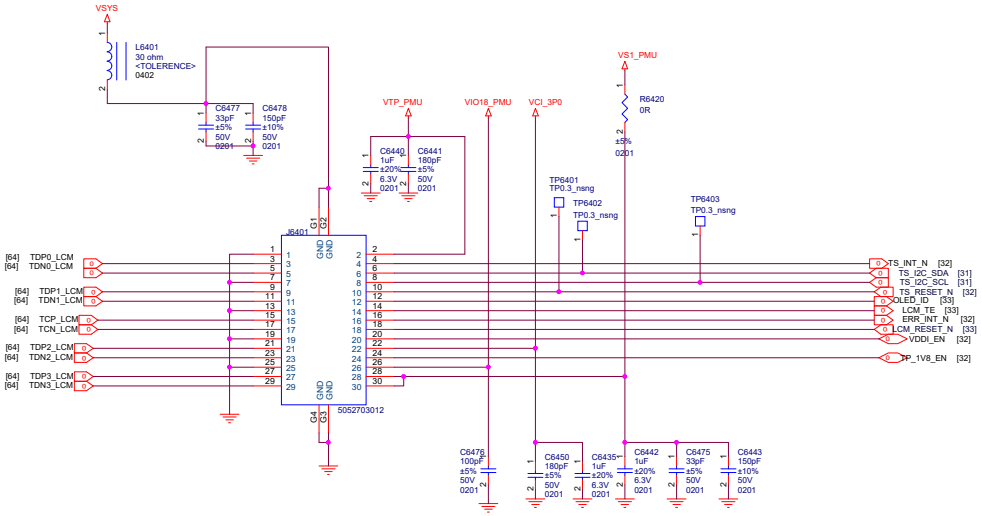

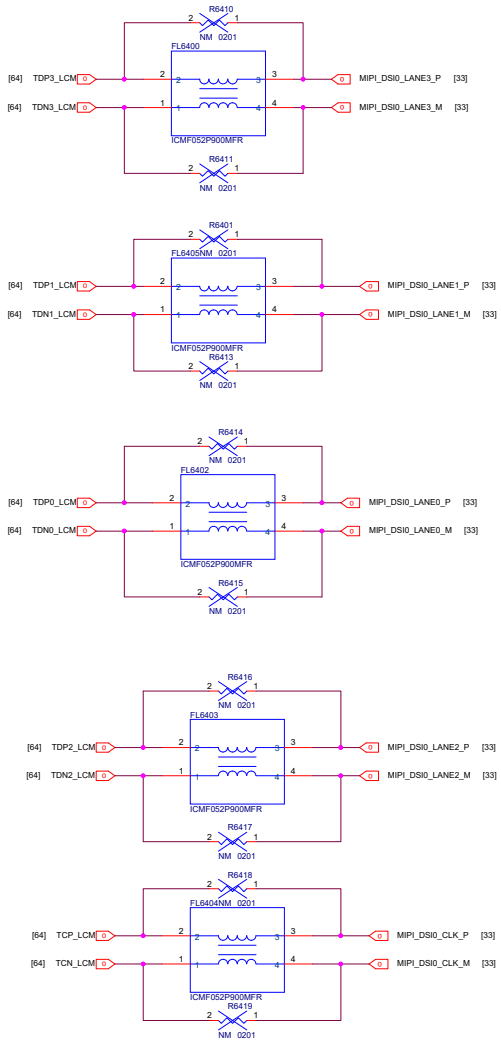

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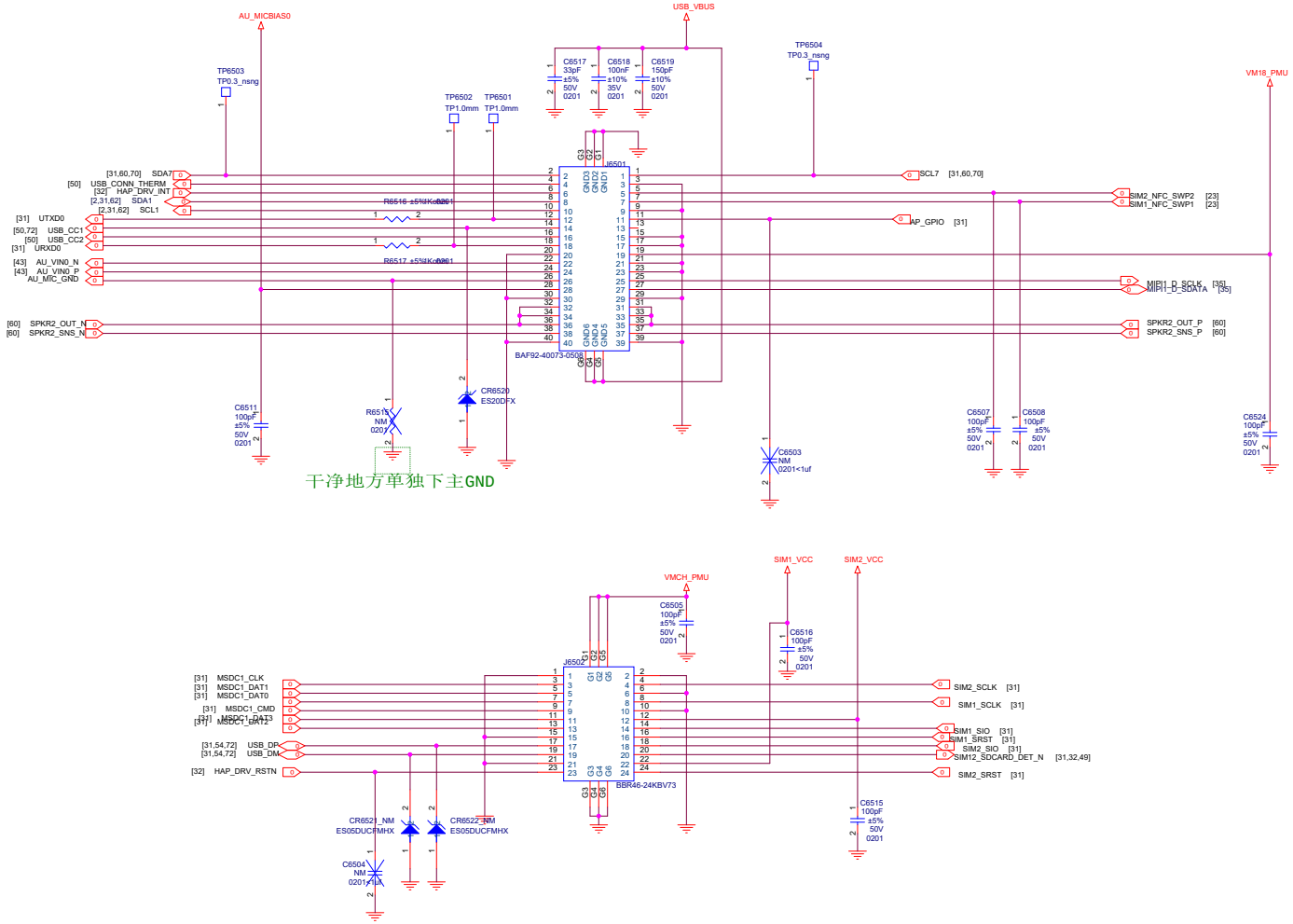
BTB CONNECTOR



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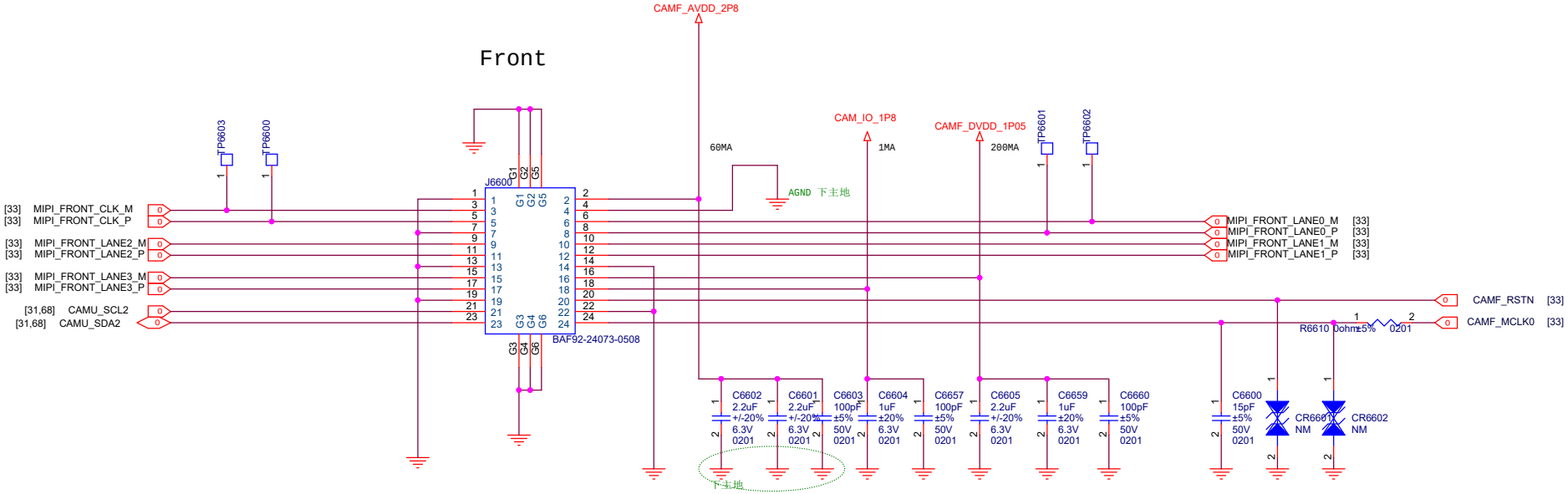

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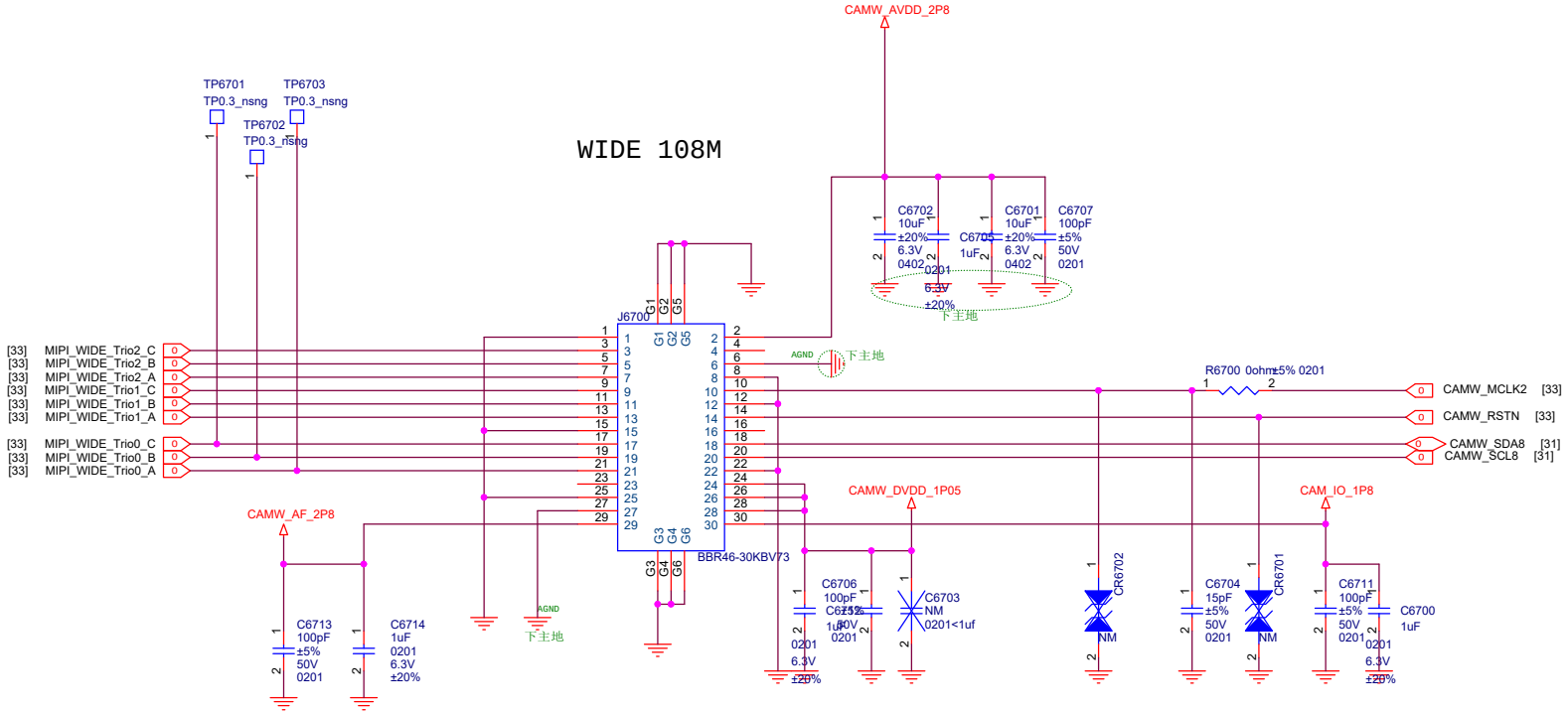

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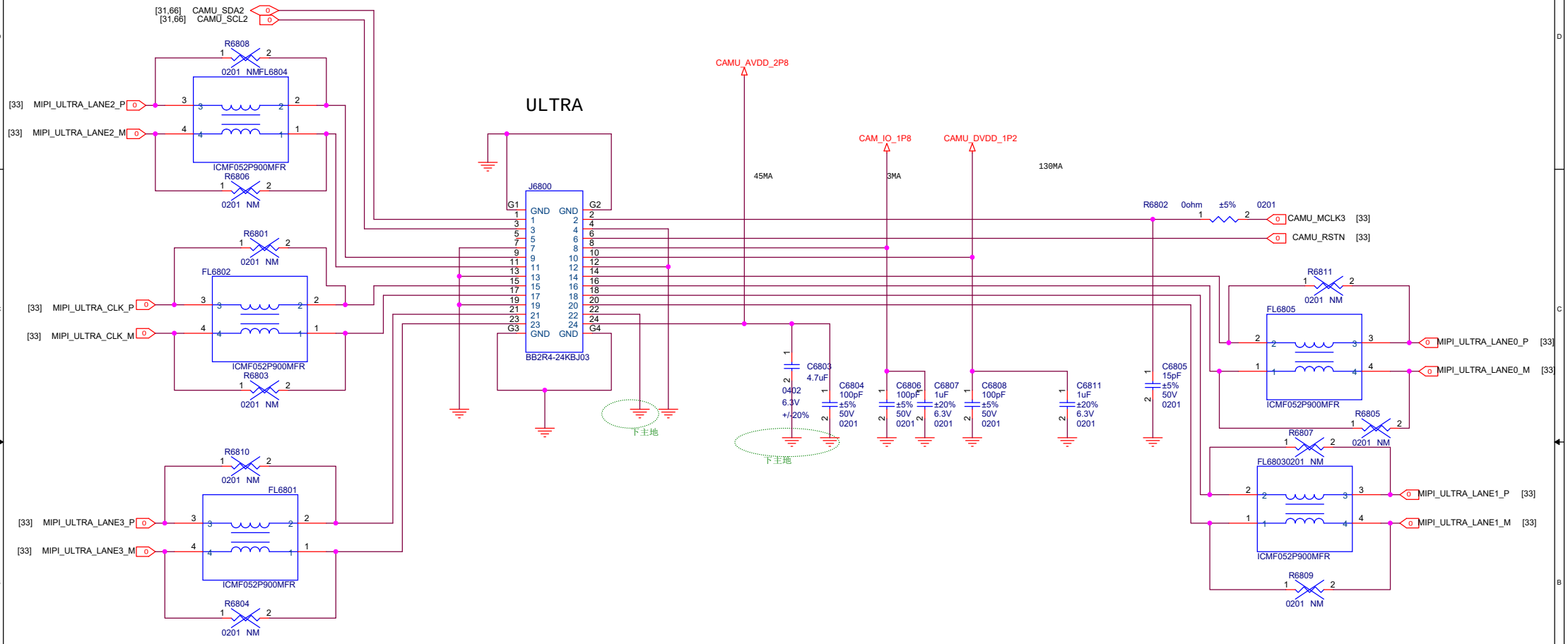

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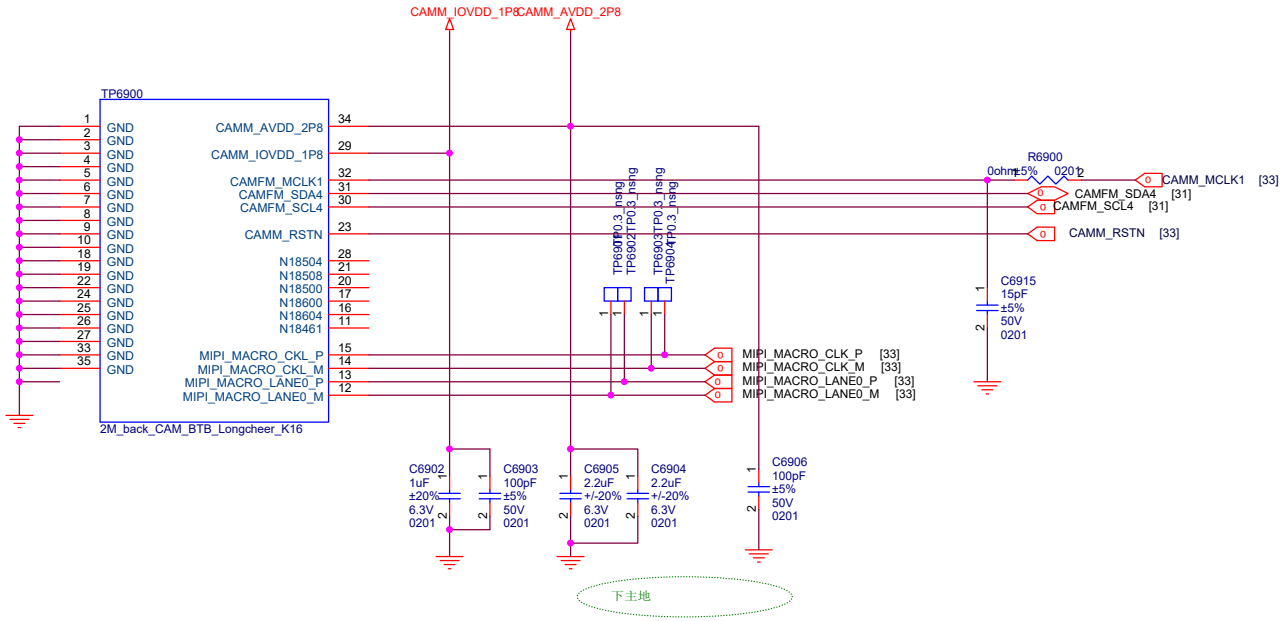
2M MACRO



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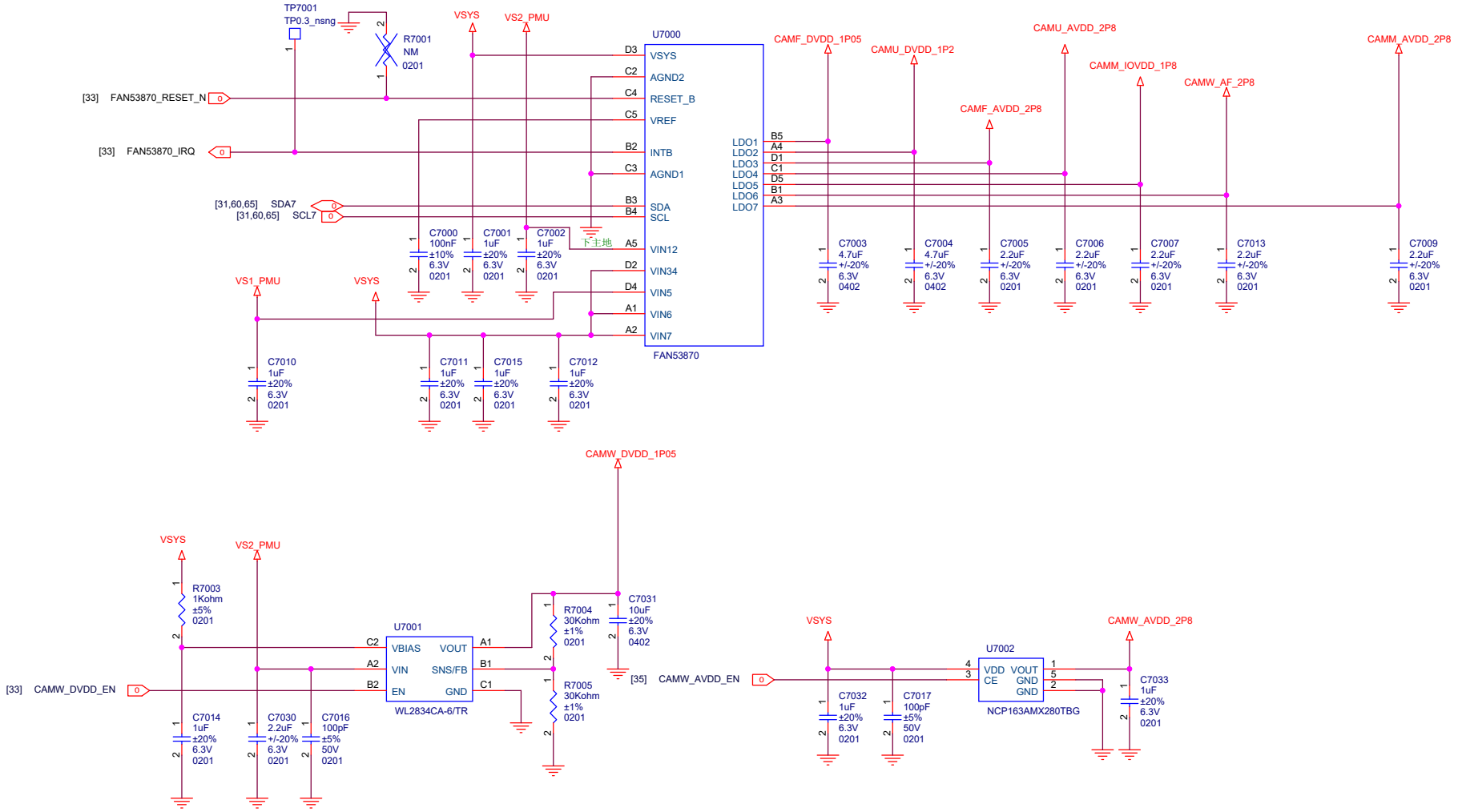

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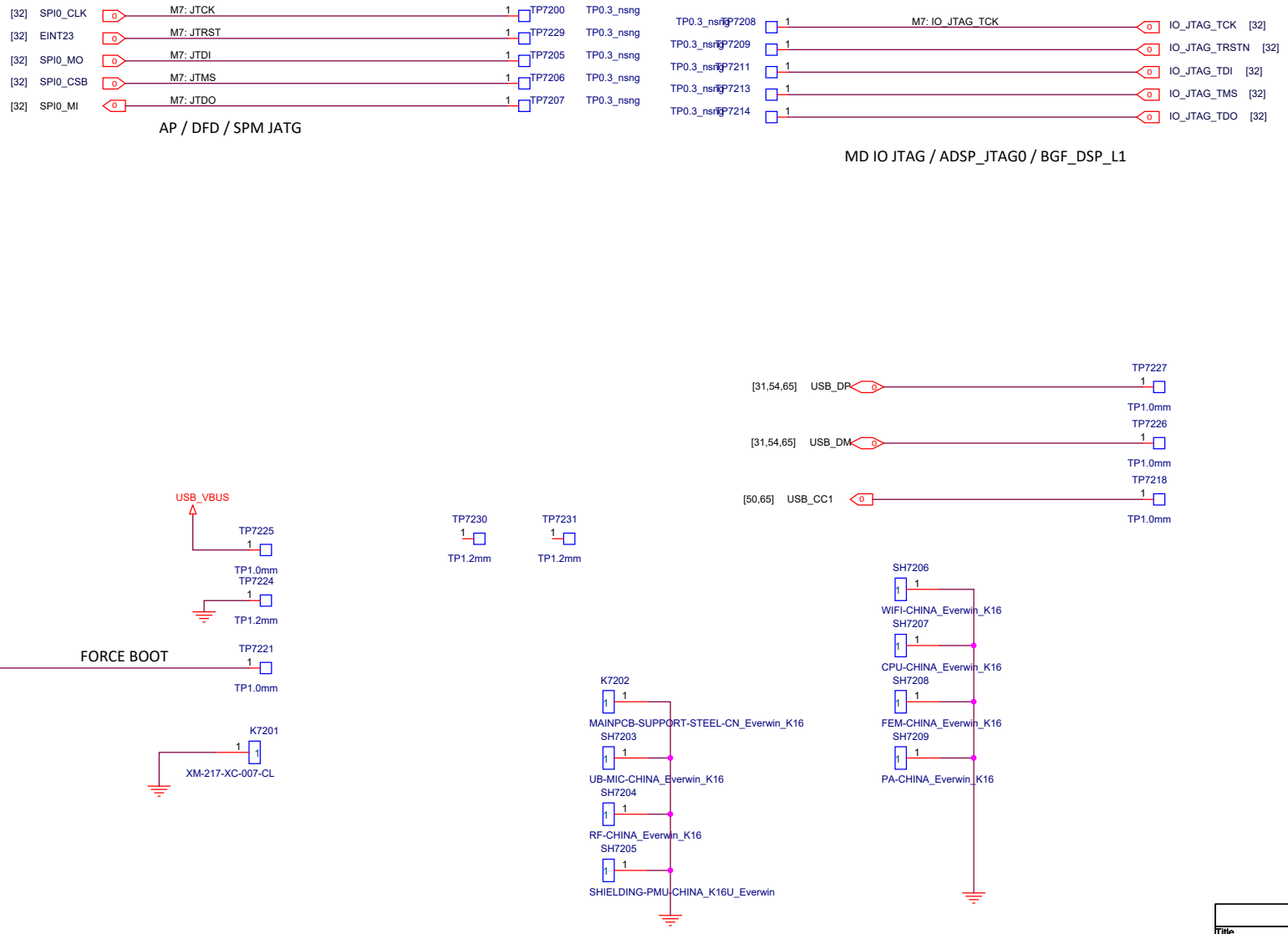
Schematic design notice of "90_DEBUG_IO" page.

Note 90-1: UART Default support : UART0,
JTAG Default support : AP JTAG/MD_IO_JTAG



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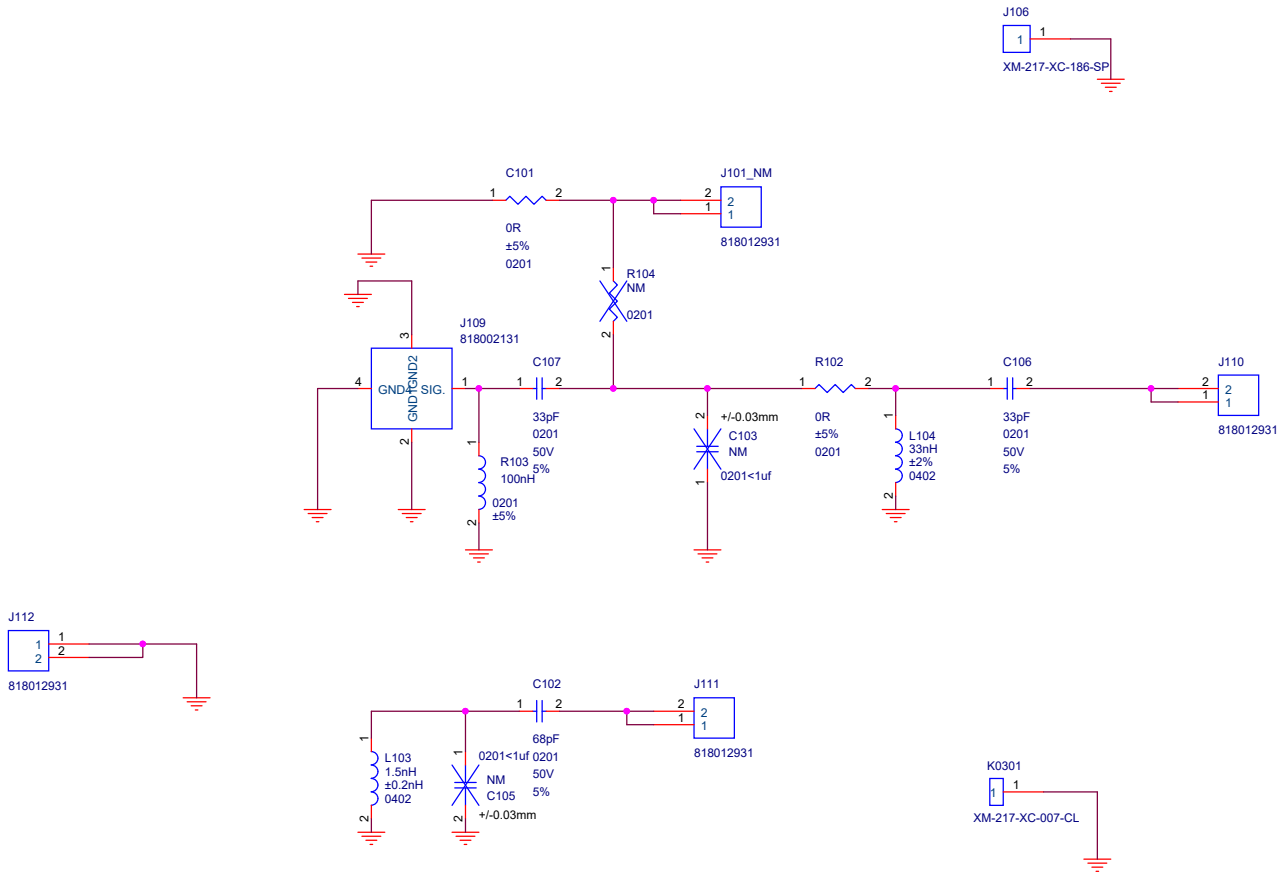

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